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(19) **United States**(12) **Patent Application Publication**
Choi et al.(10) **Pub. No.: US 2009/0121982 A1**(43) **Pub. Date: May 14, 2009**(54) **ORGANIC LIGHT EMITTING DIODE
DISPLAY AND METHOD FOR
MANUFACTURING THE SAME****Publication Classification**(51) **Int. Cl.****G09G 3/30** (2006.01)**H01L 21/00** (2006.01)**H01J 1/62** (2006.01)(52) **U.S. Cl. 345/76; 438/34; 313/504; 257/E21.001**

(57)

ABSTRACT

An organic light emitting device according to one or more embodiments includes a gate line, a data line intersecting the gate line, a switching thin film transistor connected to the gate line and the data line, a driving thin film transistor connected to the switching thin film transistor, and a light emitting diode (LED) connected to the driving thin film transistor. The switching thin film transistor includes a control electrode connected to the gate line, a crystalline semiconductor overlapping the control electrode, and an input electrode and an output electrode are spaced apart from each other on the crystalline semiconductor, wherein the control electrode and the gate line are respectively disposed under and on the crystalline semiconductor and include different materials.

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Nov. 9, 2007 (KR) 10-2007-0114155

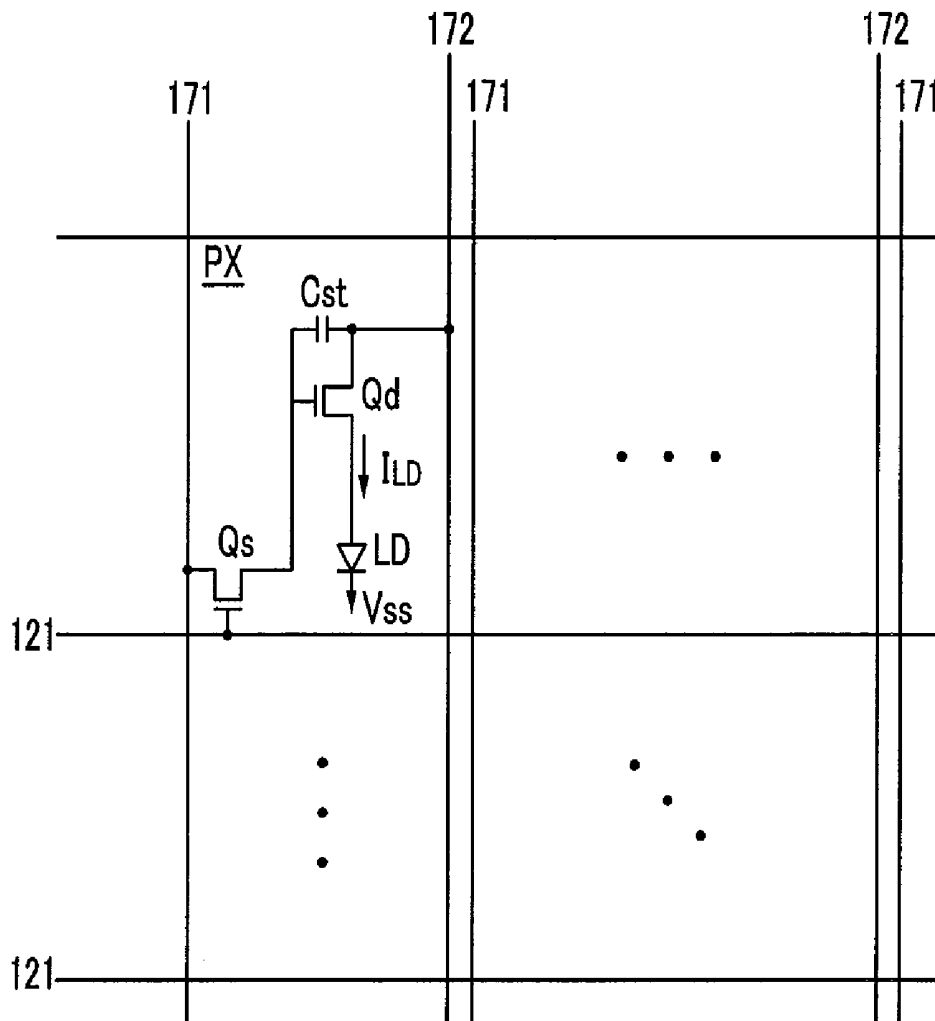


FIG.1

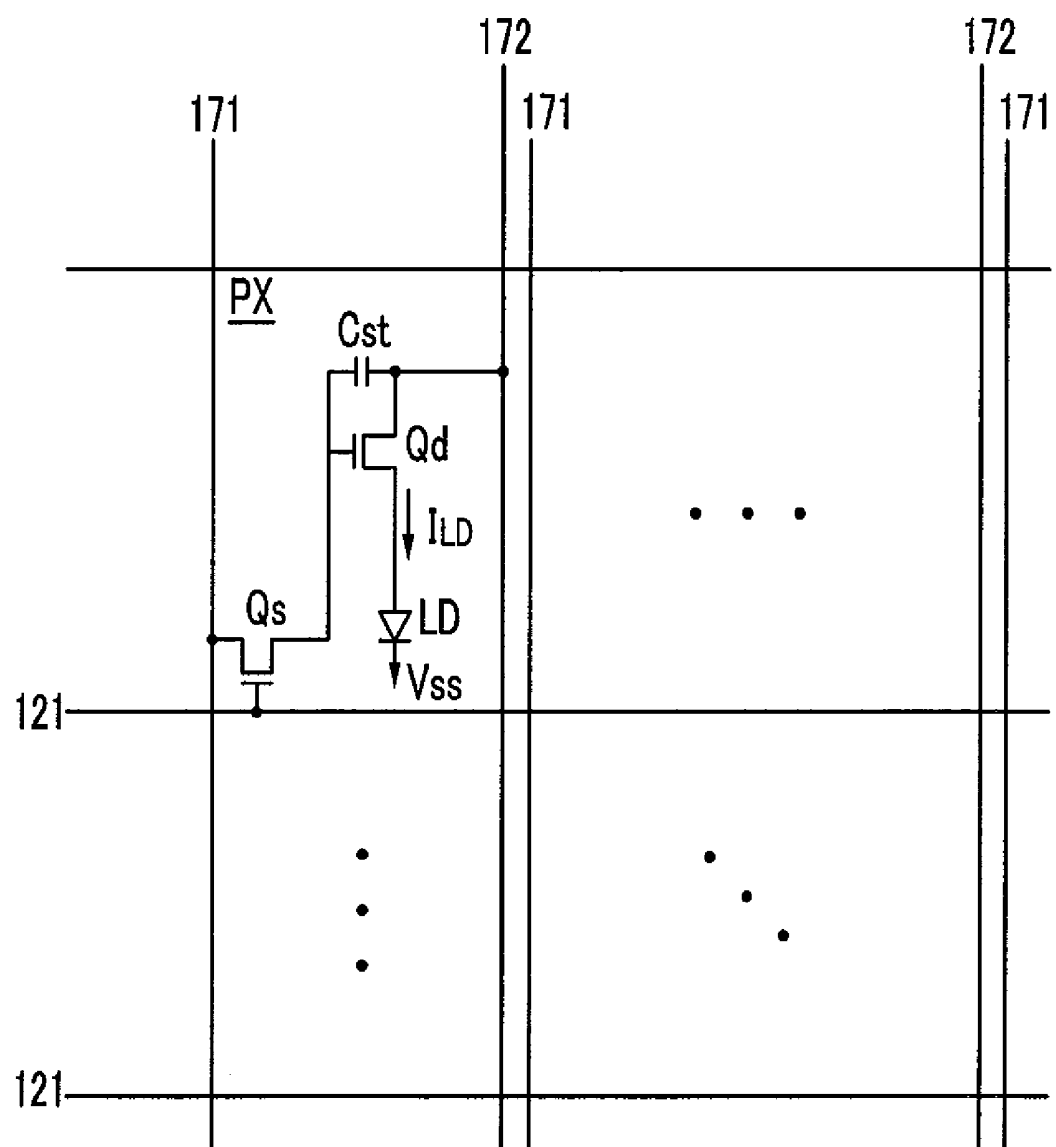


FIG.2

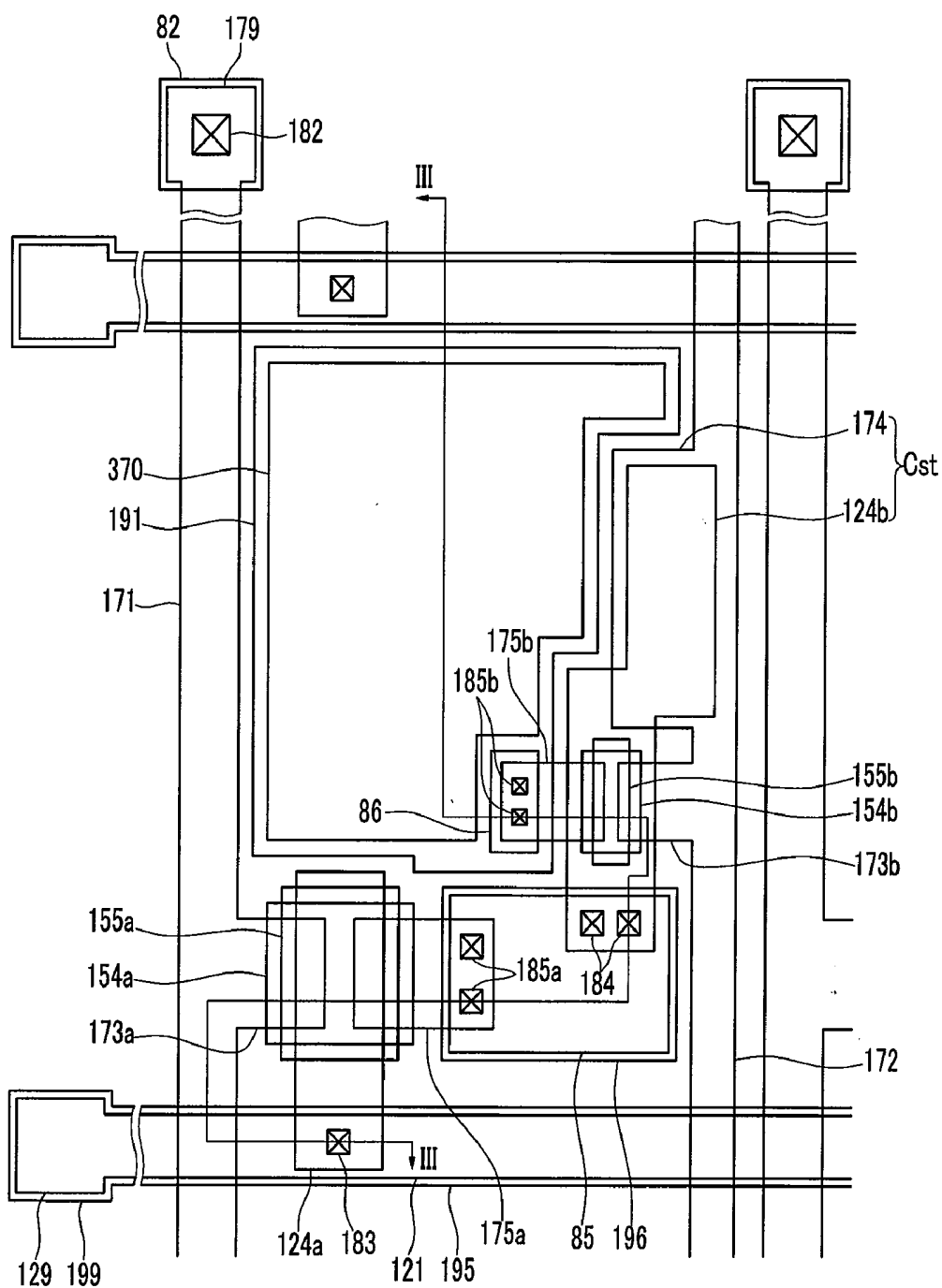


FIG.3

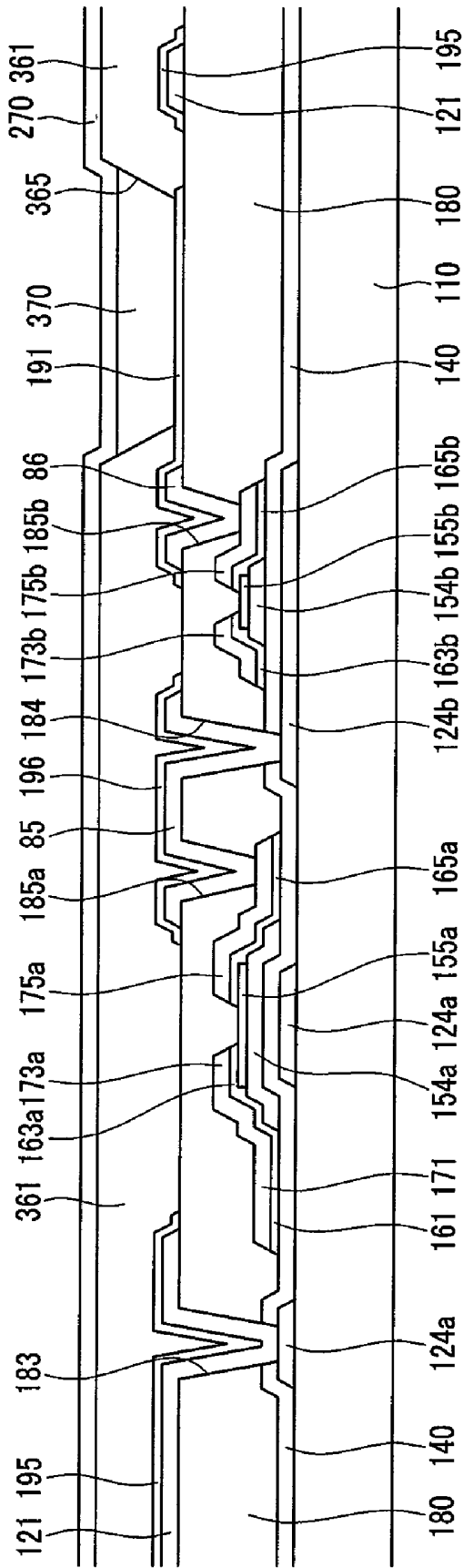


FIG.4

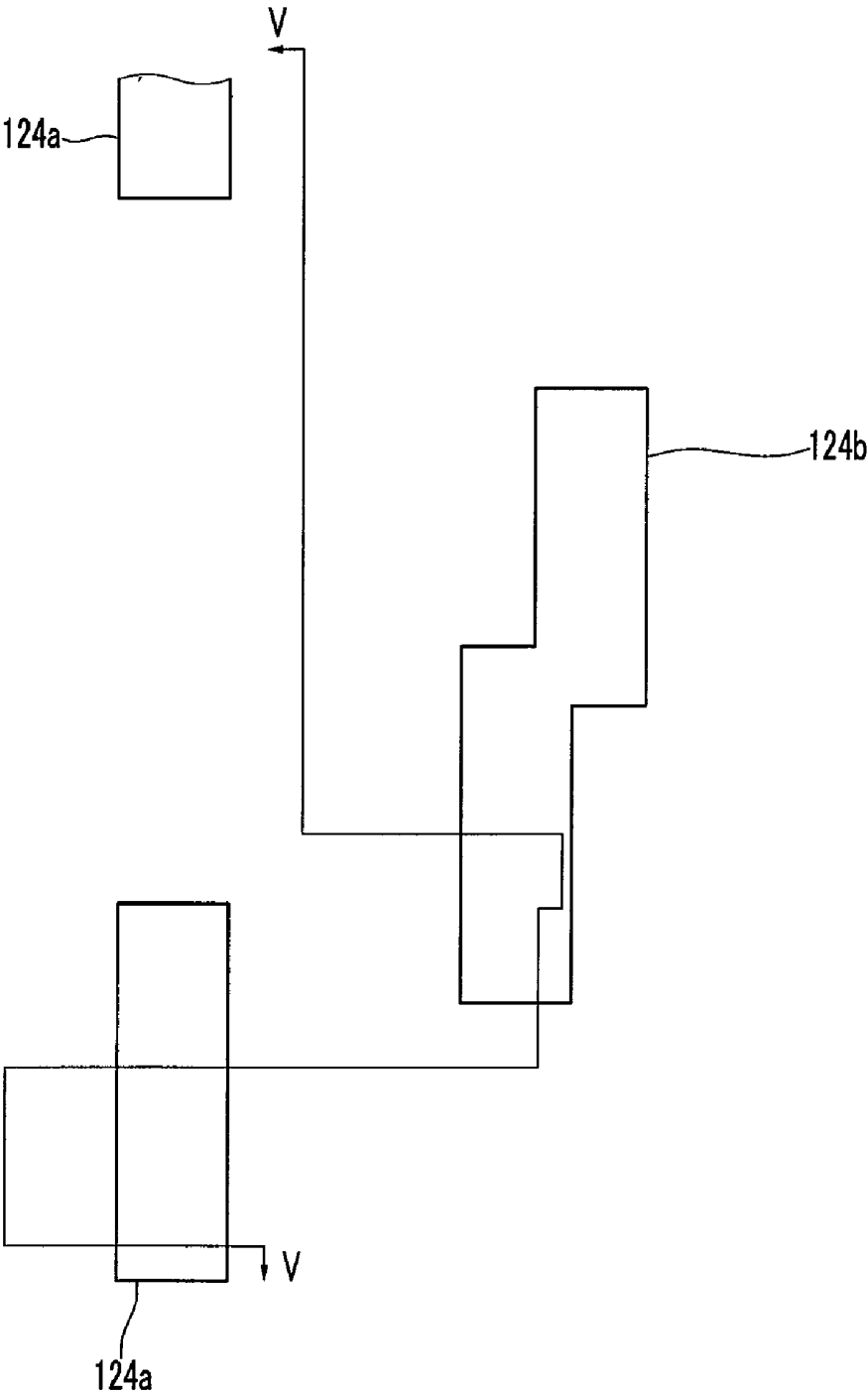


FIG.5

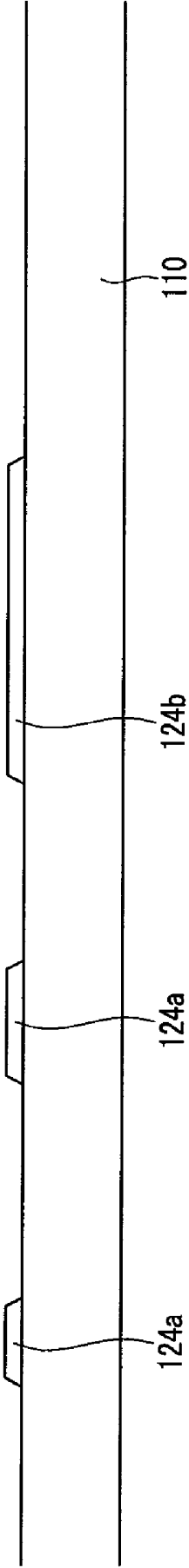


FIG.6

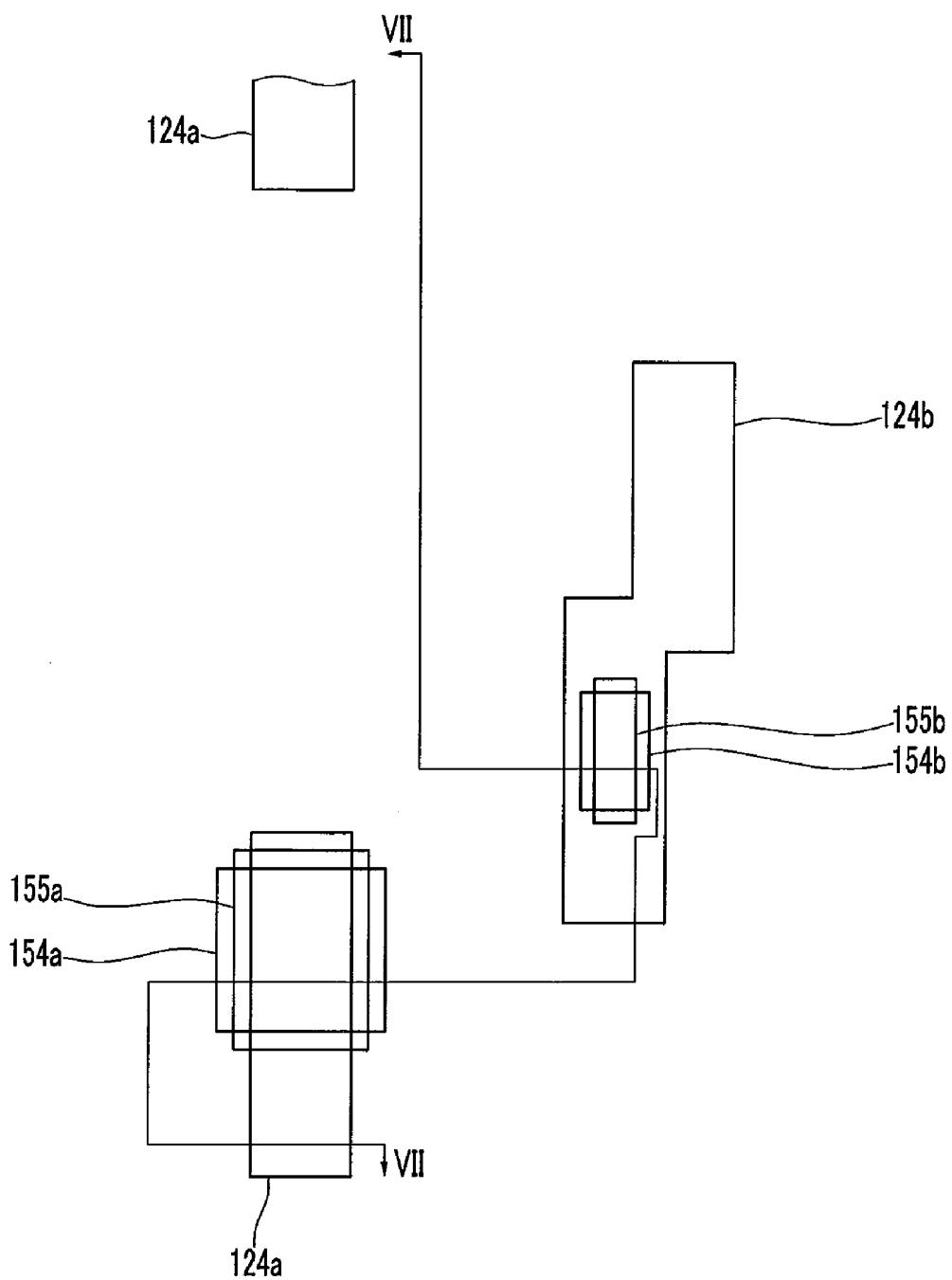


FIG. 7

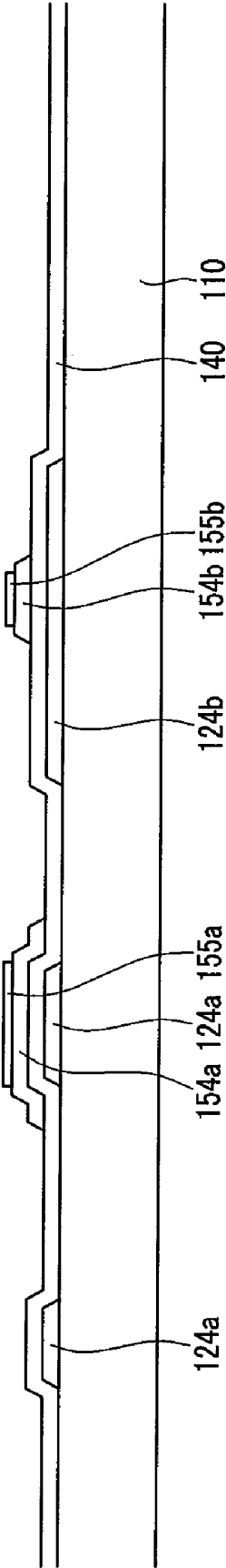


FIG. 8

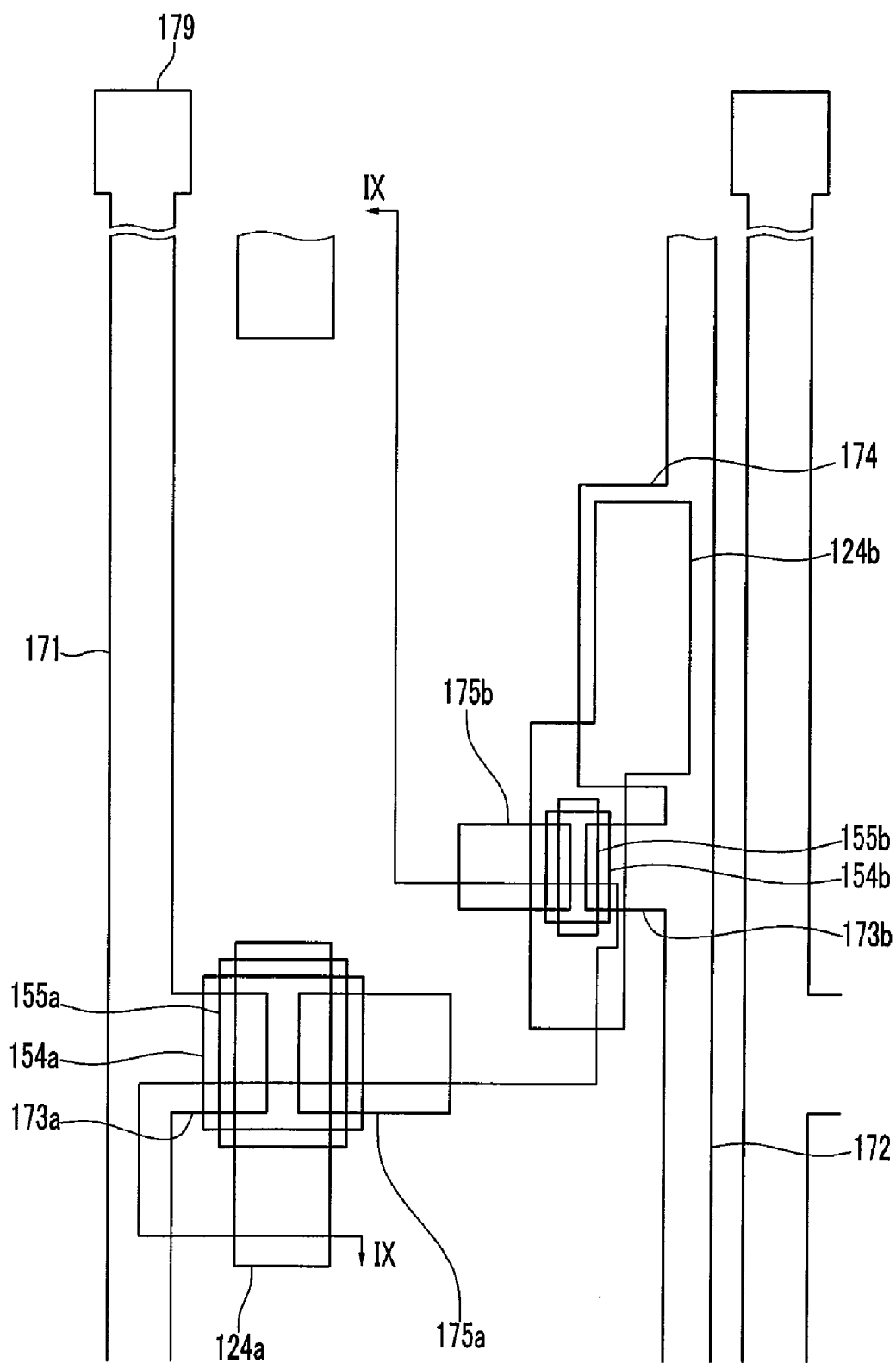


FIG. 9

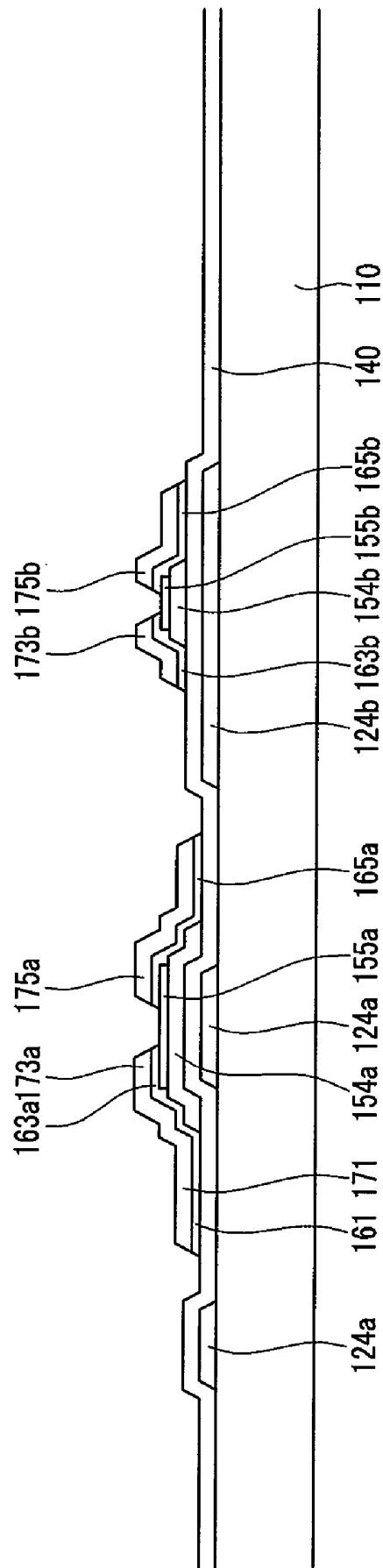


FIG.10

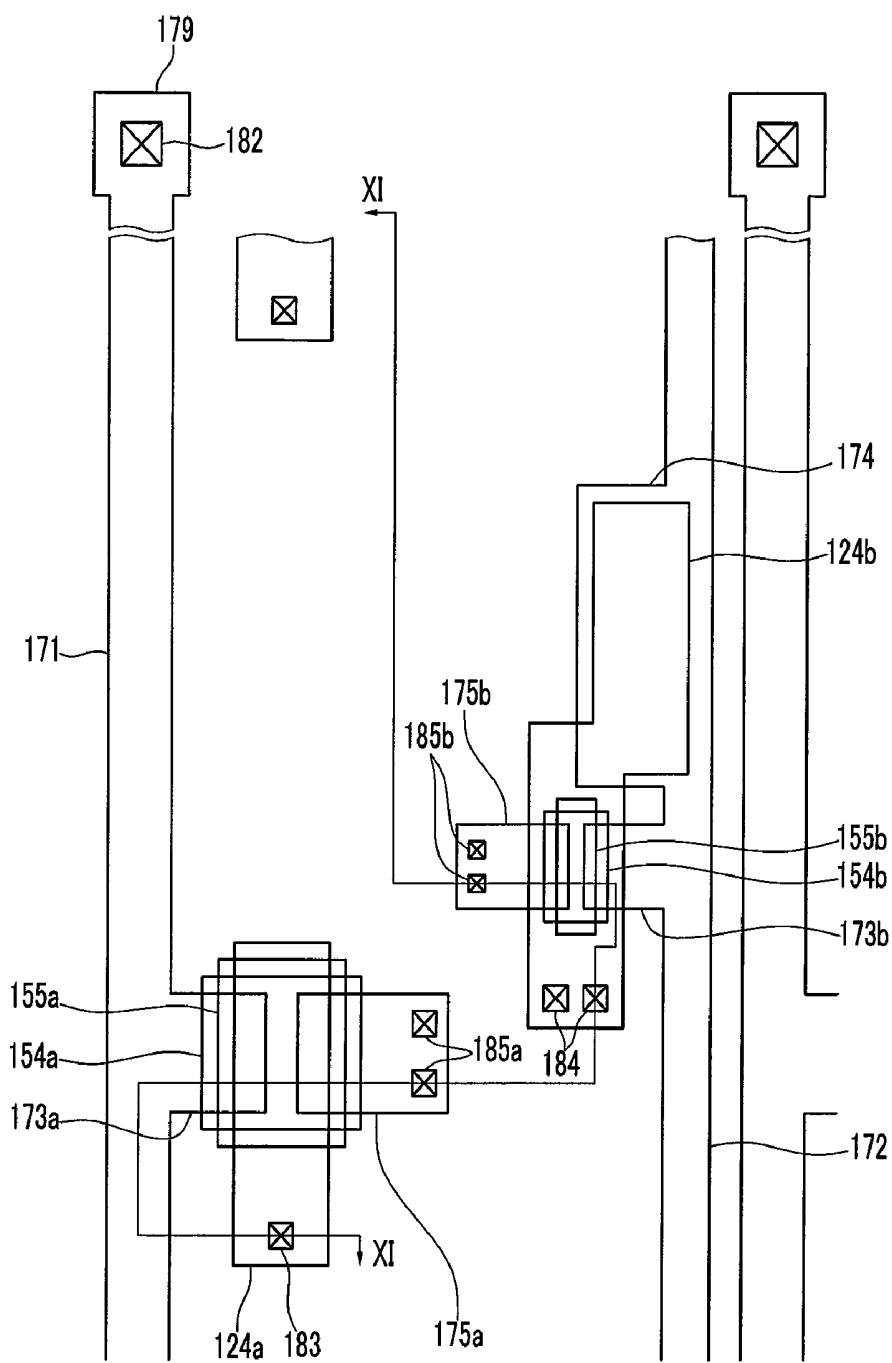
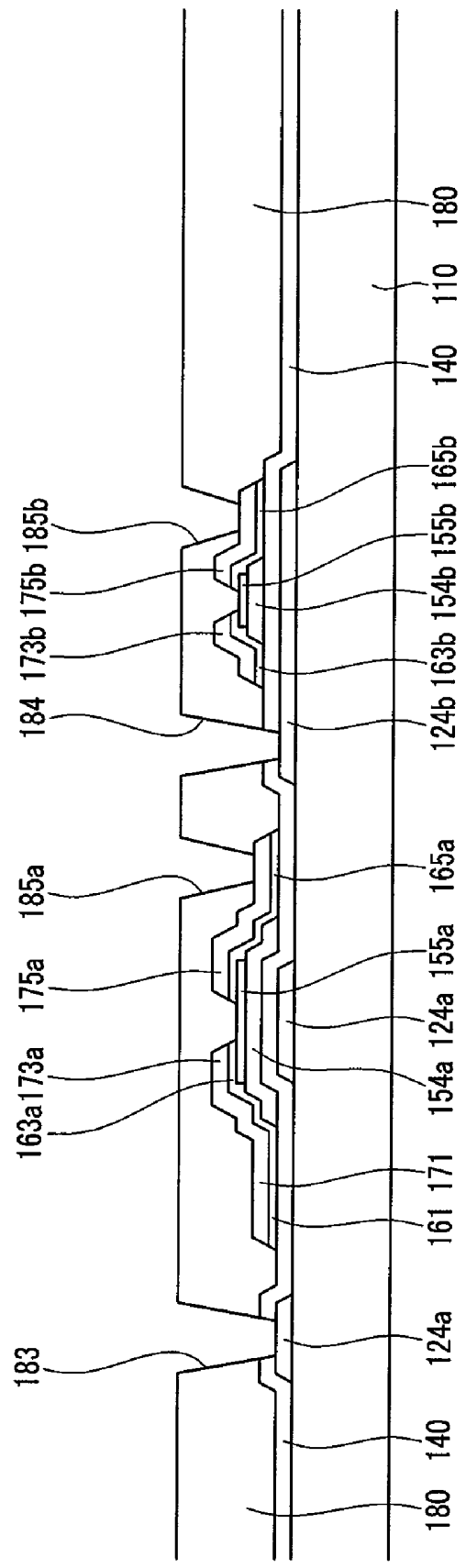


FIG.11



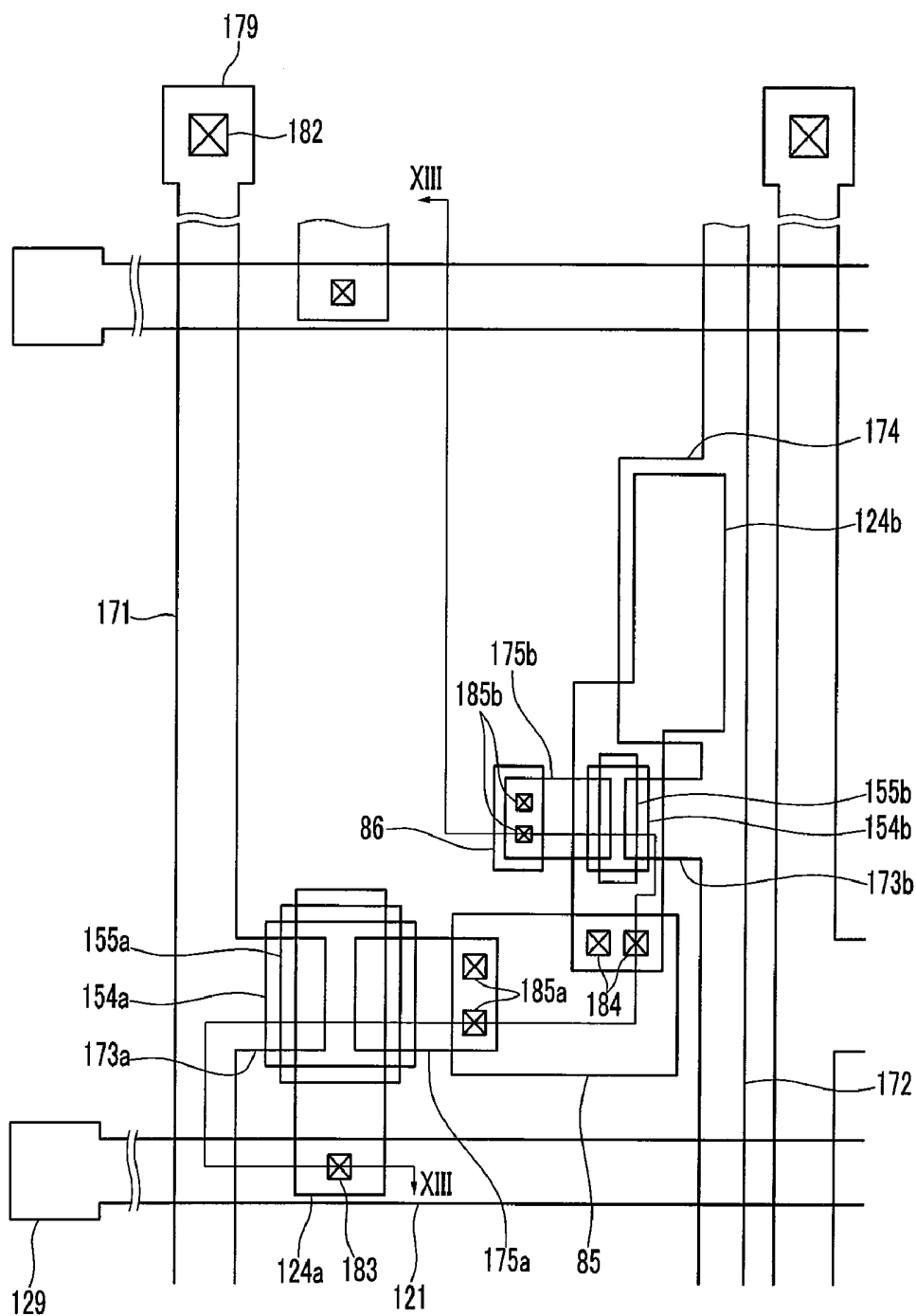


FIG.13

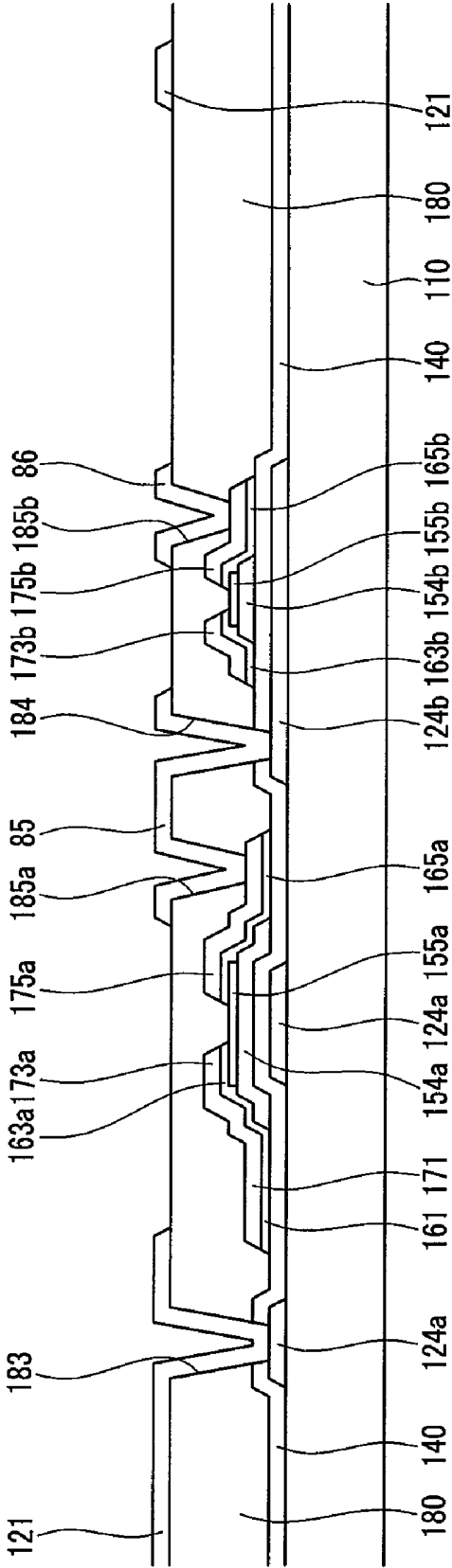


FIG.16

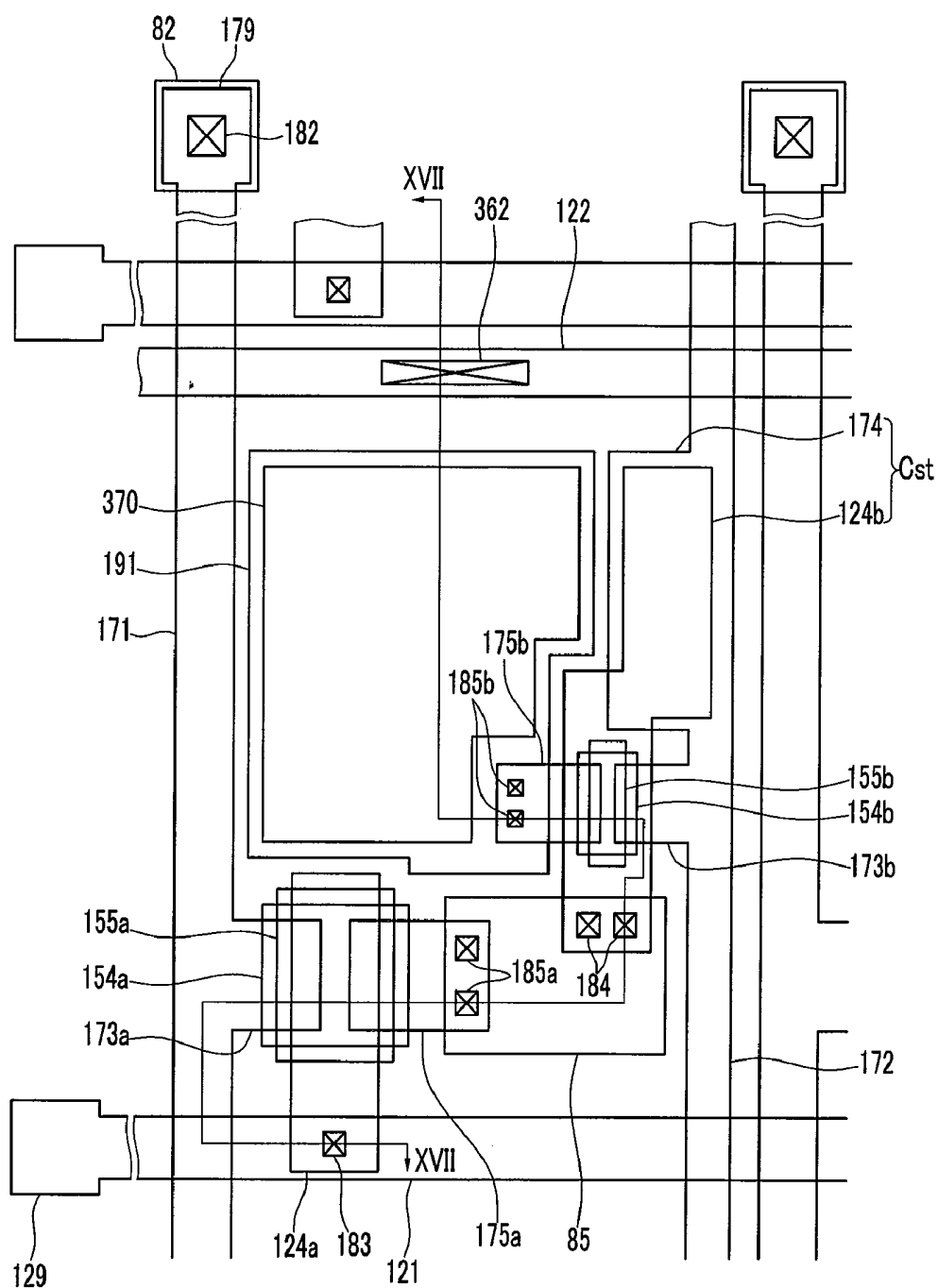


FIG.18

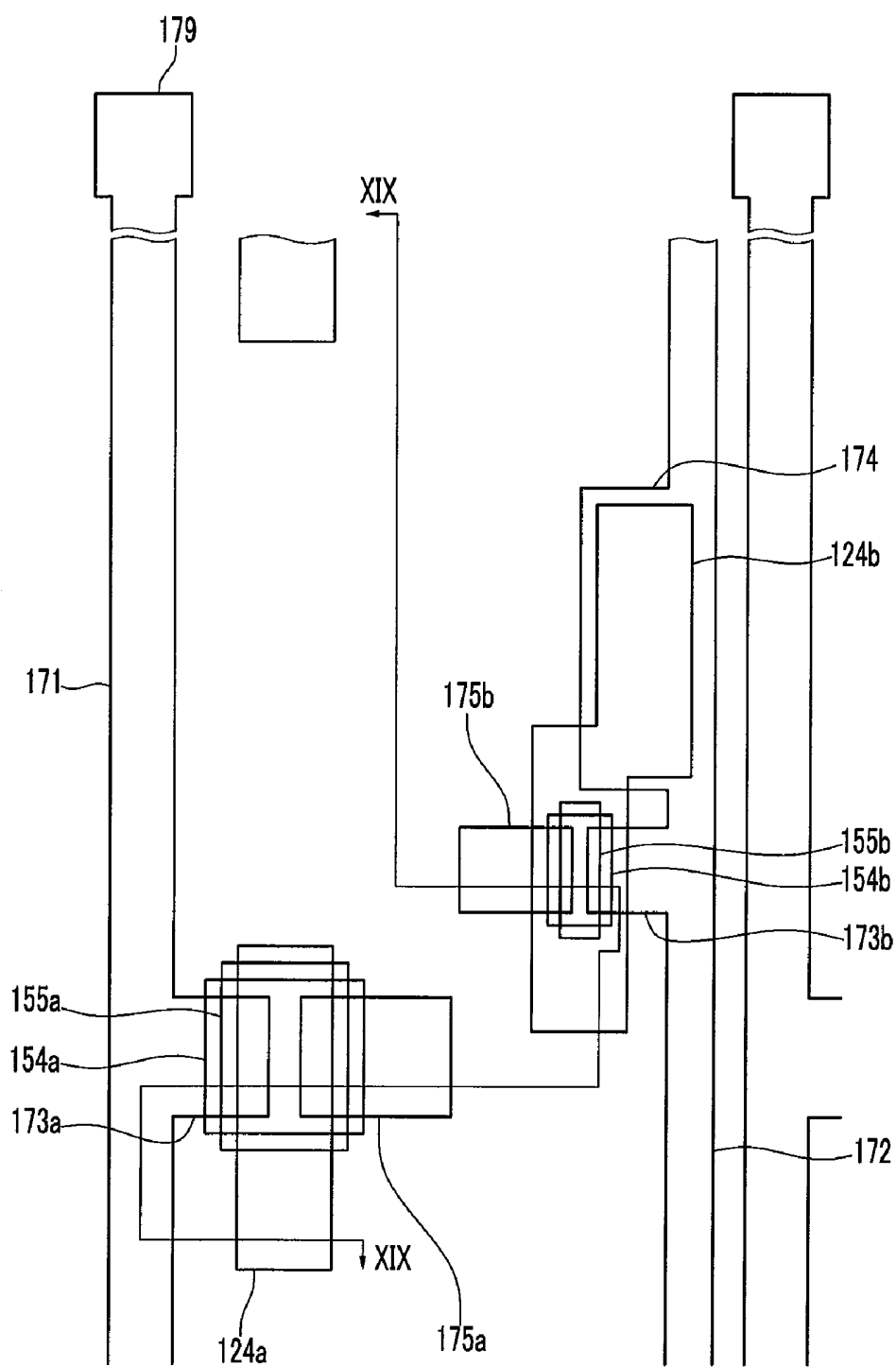


FIG. 19

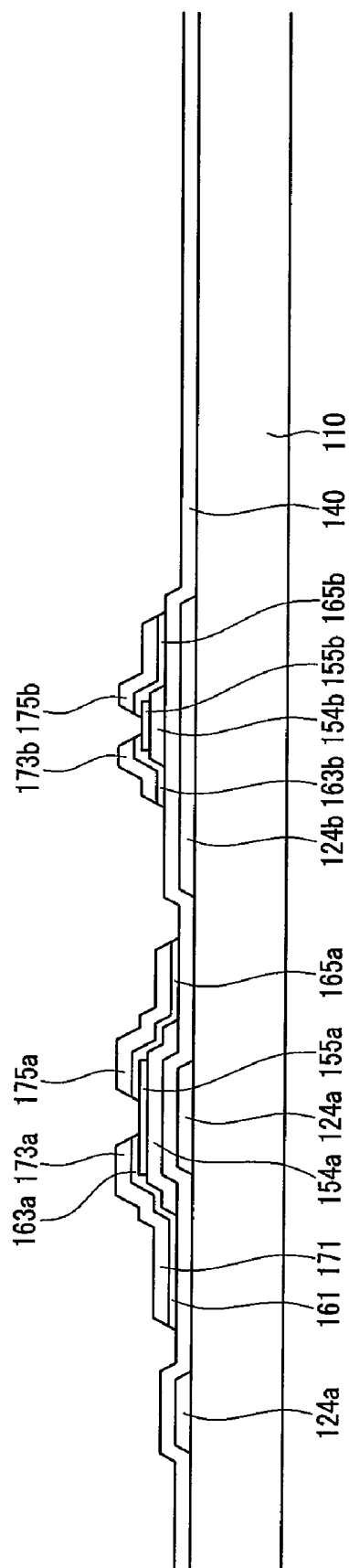


FIG.20

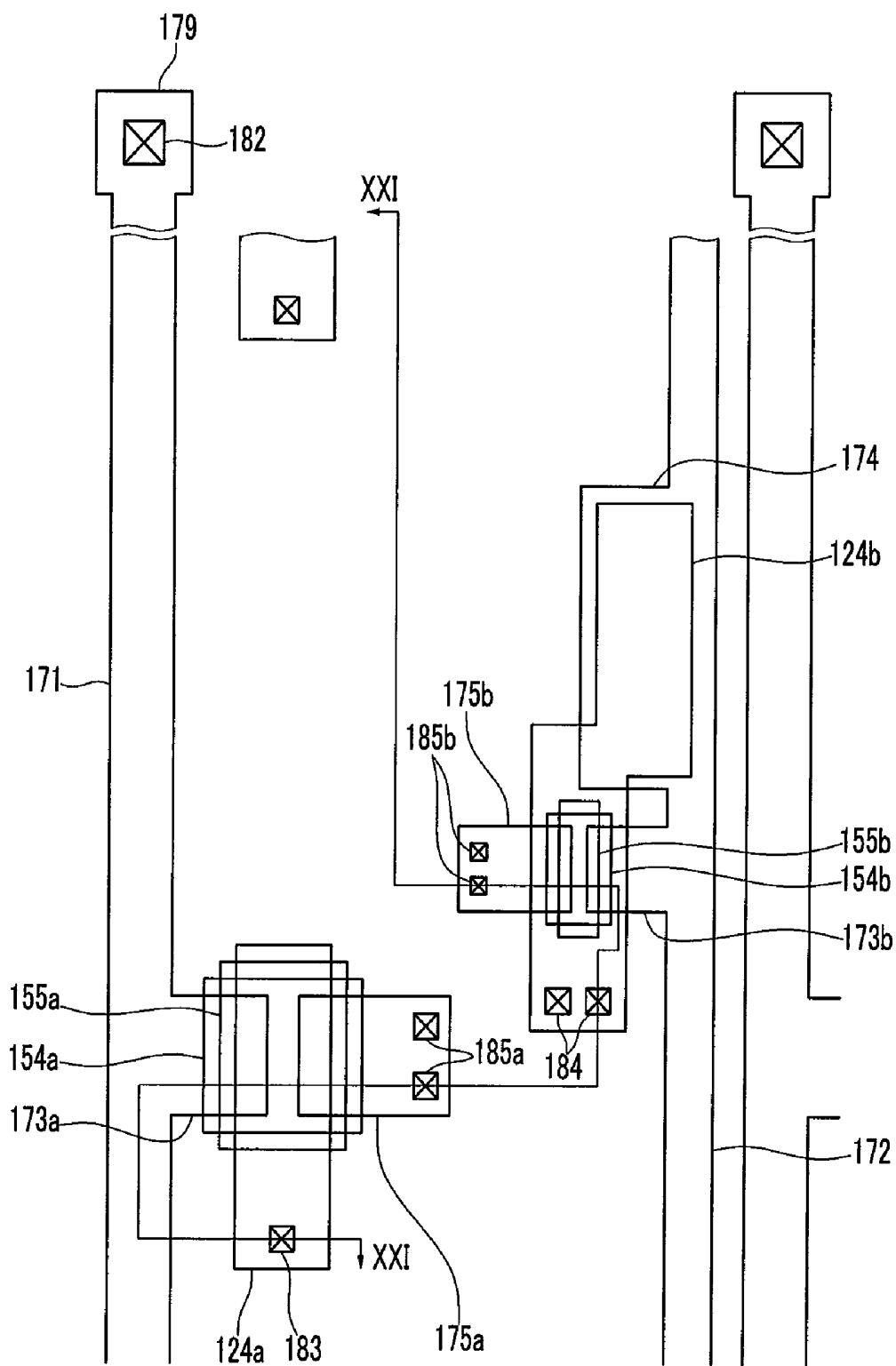


FIG. 21

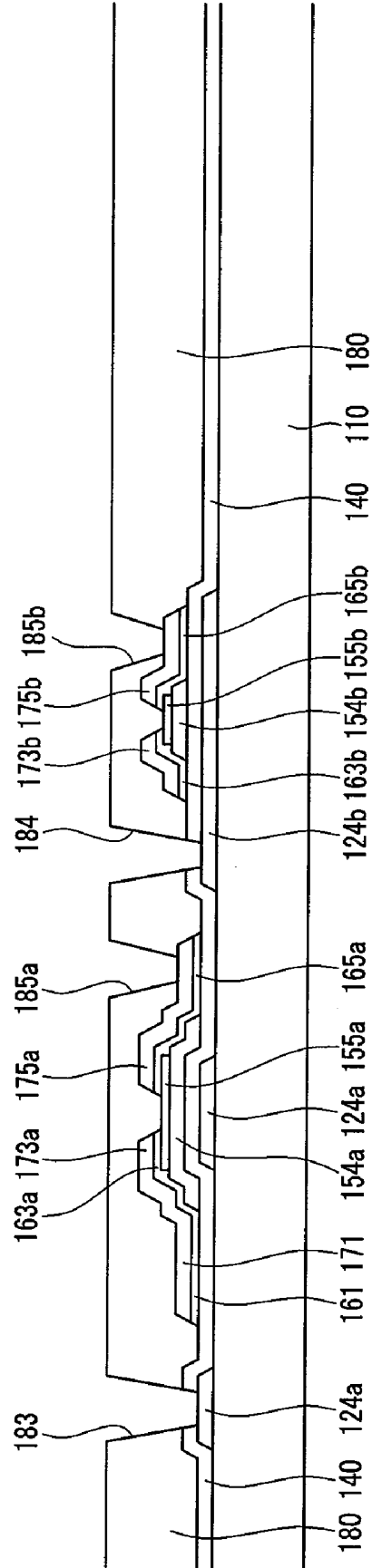


FIG.22

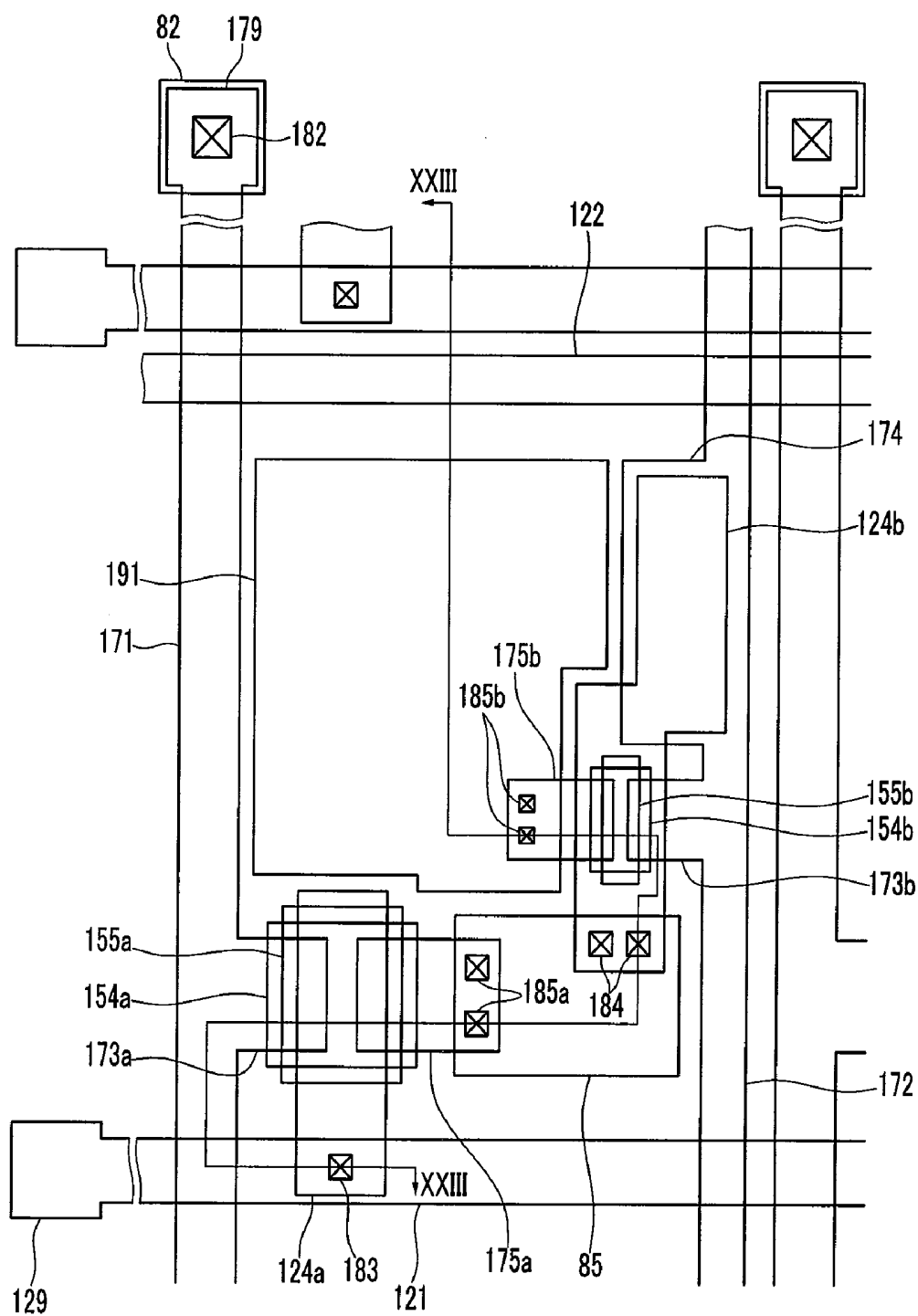


FIG.24

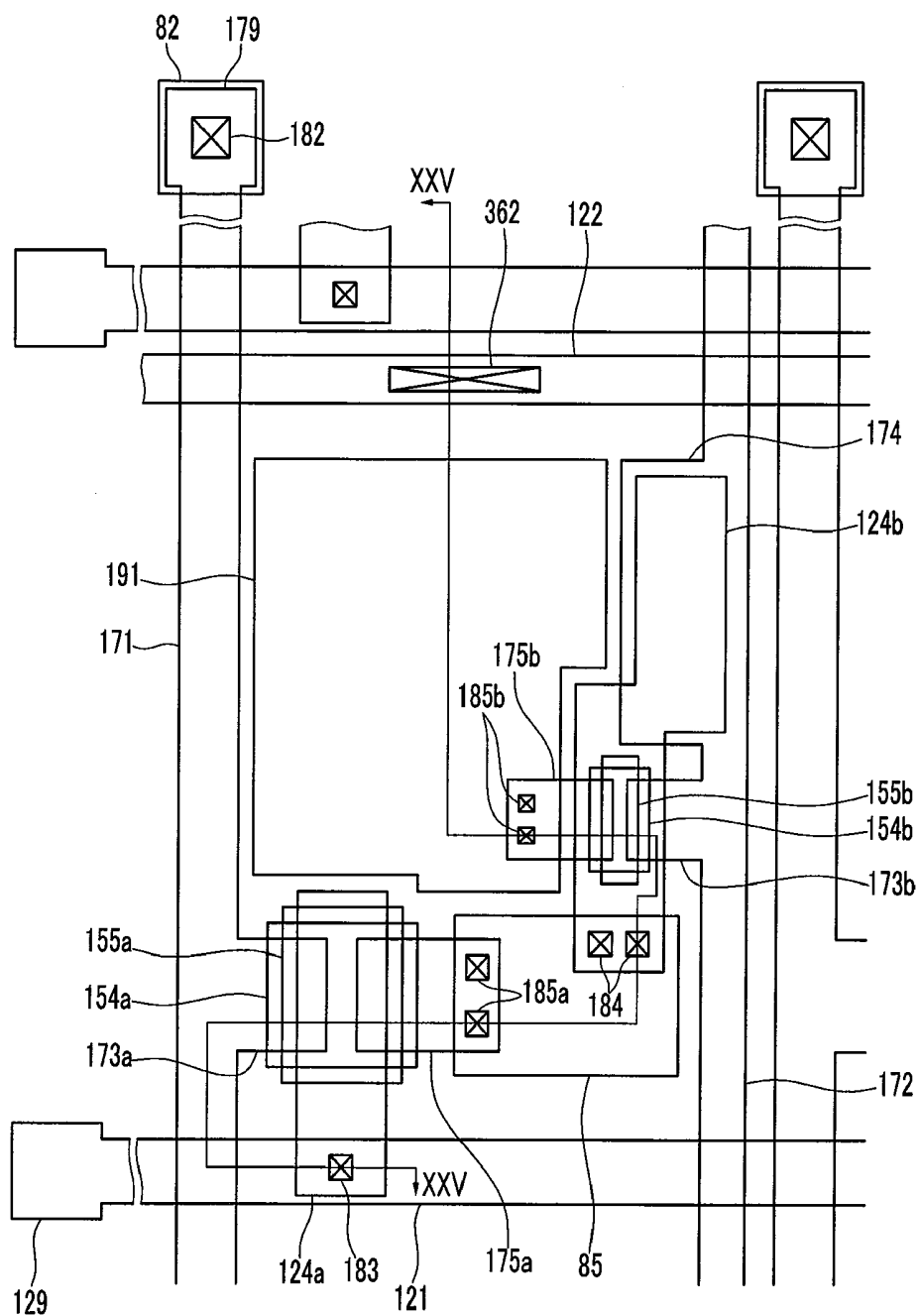
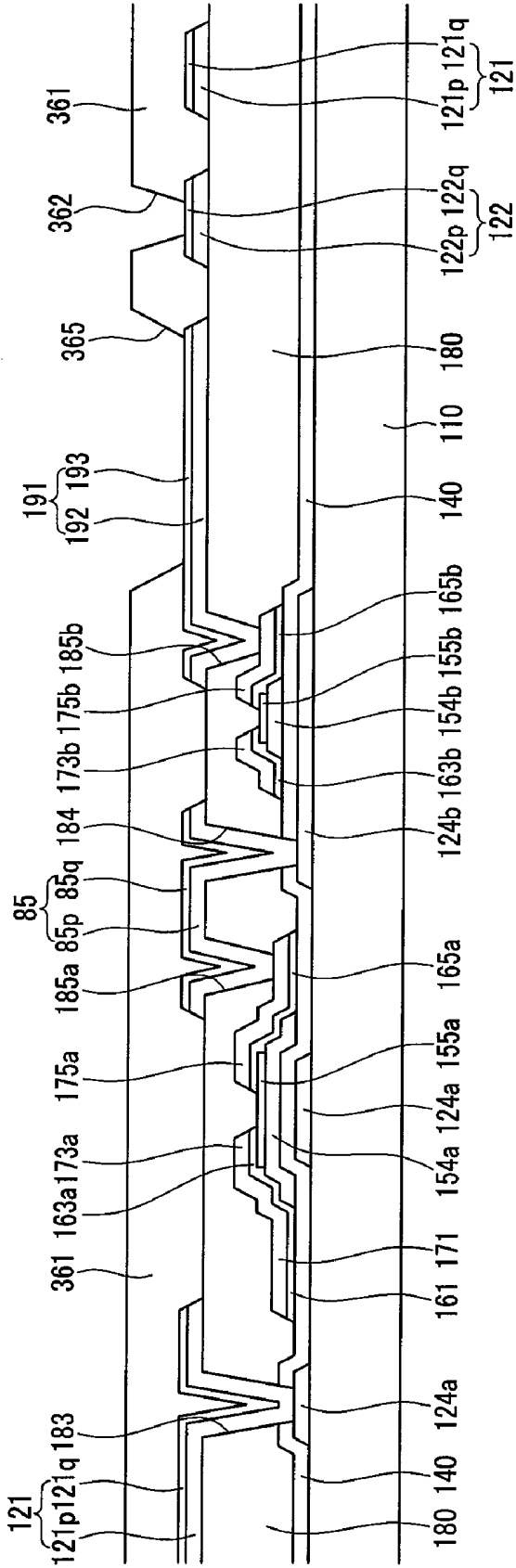


FIG.25



ORGANIC LIGHT EMITTING DIODE DISPLAY AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2007-0114155 filed in the Korean Intellectual Property Office on Nov. 9, 2007, the entire contents of which are incorporated herein by reference.

BACKGROUND

[0002] (a) Technical Field

[0003] Embodiments of the present invention relate to an organic light emitting device and a method for manufacturing the same.

[0004] (b) Description of the Related Art

[0005] Recent trends toward lightweight and thin personal computers and television sets require lightweight and thin display devices, and flat panel displays such as a liquid crystal display (LCD) that satisfy such requirements are increasingly being used in place of conventional cathode ray tubes (CRTs).

[0006] However, because the LCD is a passive display device, an additional back-light may be needed as a light source. Also, the LCD may have various problems such as a slow response time and a narrow viewing angle.

[0007] Among the flat panel displays, an organic light emitting device (organic light emitting diode display, OLED display) has recently become the most promising as a display device for solving these problems.

[0008] The OLED display includes two electrodes and an organic light emitting layer interposed between the two electrodes. One of the two electrodes injects holes and the other electrode injects electrons into the light emitting layer. The injected electrons and holes are combined to form excitons, and the excitons in turn emit light as they release energy.

[0009] Because the OLED display is a self-emissive display device, an additional light source is not necessary such that the organic light emitting device has lower power consumption as well as a high response speed, wide viewing angle, and high contrast ratio.

[0010] The OLED display may be classified as a passive matrix OLED display and an active matrix OLED display according to driving type. In the active OLED display, an electrode and an emission layer are disposed on a thin film transistor array panel. The thin film transistor array panel includes signal lines, switching thin film transistors connected to the signal lines for controlling data voltages, and driving thin film transistors directing the current to a light-emitting device by applying the transmitted data voltages as gate voltages.

[0011] Also, the OLED display may be classified as a bottom emission type and a top emission type according to the direction of emission. In the bottom emission type, the light emitted from the emission layer passes through a thin film transistor array panel to exit the display. In contrast, in the top emission type, the light emitted from the emission layer passes through a common electrode to exit the display. For a high aperture ratio, the top emission type may be used because an aperture ratio of the top emission type is not influenced by the presence of the signal lines and the thin film transistors.

[0012] In an active matrix OLED display, high mobility, high stability, and uniformity of the thin film transistor are required. To satisfy these characteristics, a bottom gate structure using a polysilicon as a semiconductor may be considered, but because the process of high temperature crystallization of an amorphous silicon is required, the gate metal is limited to using a material having a high melting point. However, a signal line having low resistivity must be used to prevent, for example, a signal delay in a large-sized OLED display, but because a low resistivity material for signal lines has a low melting point, such material may not be used as the gate metal.

[0013] Also, while the OLED display of the top emission type may obtain a high aperture ratio, the common electrode must be made of a transparent conductive material. However, because the transparent conductive material has a high resistivity, a drop in the common voltage may be generated.

SUMMARY

[0014] Systems and methods are disclosed, in accordance with one or more embodiments, to reduce a signal delay, to improve the characteristics of a thin film transistor, and to prevent a voltage drop of the common voltage in an organic light emitting device of a top emission type.

[0015] An organic light emitting diode (OLED) display according to an exemplary embodiment of the present invention includes a gate line, a data line intersecting the gate line, a switching thin film transistor connected to the gate line and the data line, a driving thin film transistor connected to the switching thin film transistor, and a light emitting diode (LED) connected to the driving thin film transistor. The switching thin film transistor includes a control electrode connected to the gate line, a crystalline semiconductor overlapping the control electrode, and an input electrode and an output electrode are spaced apart from each other on the crystalline semiconductor, wherein the control electrode and the gate line are respectively disposed under and on the crystalline semiconductor and include different materials.

[0016] According to an embodiment, the gate line may include a metal having a melting point less than that of the control electrode. For example, the gate line may include one selected from an aluminum-containing metal, a copper-containing metal, and a silver-containing metal, and the control electrode may include one selected from a molybdenum-containing metal, a chromium-containing metal, a titanium-containing metal, a tantalum-containing metal, and a tungsten-containing metal.

[0017] According to an embodiment, the light emitting diode (LED) may include a first electrode connected to the driving thin film transistor, a second electrode spaced apart from the first electrode, and a light emitting member disposed between the first electrode and the second electrode, wherein the first electrode may be disposed on the same layer as the gate line.

[0018] The first electrode may include, according to an embodiment, a first layer including a metal and a second layer including a transparent conductive material, wherein the second layer may contact the light emitting member. The first electrode and the gate line may be formed on the same layer, and a voltage assistant line may be connected to the second electrode.

[0019] In an embodiment, the OLED display may further include an organic insulating layer formed on the first electrode, wherein the organic insulating layer may have an open-

ing defining the light emitting member and a contact hole exposing the voltage assistant line.

[0020] In an embodiment, the light emitting diode (LED) may include a first electrode connected to the driving thin film transistor, a second electrode spaced apart from the first electrode, and a light emitting member disposed between the first electrode and the second electrode, and may further include a first protecting member formed on the same layer as the first electrode and covering the gate line.

[0021] In another embodiment, the OLED display may further include a connecting member connecting the driving thin film transistor and the switching thin film transistor, and may be formed on the same layer as the gate line. The OLED display may further include a second protecting member formed on the same layer as the first electrode and covering the connecting member.

[0022] An OLED display according to another exemplary embodiment of the present invention includes: a first control electrode and a second control electrode formed on a substrate; a first crystalline semiconductor and a second crystalline semiconductor formed on the first control electrode and the second control electrode; a first input electrode and a first output electrode spaced apart from each other on the first crystalline semiconductor; a second input electrode and a second output electrode spaced apart from each other on the second crystalline semiconductor; an insulating layer formed on the first input electrode, the first output electrode, the second input electrode, and the second output electrode, and having a first contact hole exposing the first control electrode, a second contact hole exposing the first output electrode, a third contact hole exposing the second control electrode, and a fourth contact hole exposing the second output electrode; a gate line formed on the insulating layer and connected to the first control electrode through the first contact hole; a pixel electrode connected to the second output electrode through the fourth contact hole; a common electrode facing the pixel electrode; and a light emitting member disposed between the pixel electrode and the common electrode.

[0023] According to an embodiment, the gate line may include a metal having a lower melting point than that of the first control electrode. For example, the gate line may include one selected from an aluminum-containing metal, a copper-containing metal, and a silver-containing metal, and the first control electrode may include one selected from a molybdenum-containing metal, a chromium-containing metal, a titanium-containing metal, a tantalum-containing metal, and a tungsten-containing metal. The gate line and the pixel electrode may be formed on the same layer.

[0024] In an embodiment, the OLED display may further include a connecting member connecting the first output electrode and the second control electrode to each other through the second contact hole and the third contact hole, wherein the connecting member is formed on the same layer as the gate line and the pixel electrode. The OLED display according to an embodiment may further include a voltage assistant line connected to the common electrode, wherein the voltage assistant line is formed on the same layer as the gate line, the pixel electrode, and the connecting member. In another embodiment, the OLED display may further include a voltage assistant line connected to the common electrode, wherein the voltage assistant line is formed on the same layer as the gate line and the pixel electrode.

[0025] A method for manufacturing an OLED display according to an exemplary embodiment of the present inven-

tion includes: forming a first control electrode and a second control electrode on a substrate; forming a first crystalline semiconductor and a second crystalline semiconductor on the first control electrode and the second control electrode; forming the first input electrode and the first output electrode facing each other on the first crystalline semiconductor, and forming the second input electrode and the second output electrode facing each other on the second crystalline semiconductor; forming an insulating layer on the first input electrode, the first output electrode, the second input electrode, and the second output electrode; forming a gate line connected to the first control electrode on the insulating layer; forming a pixel electrode on the insulating layer; forming a light emitting member on the pixel electrode; and forming a common electrode on the light emitting member.

[0026] According to an embodiment, the forming of the first crystalline semiconductor and the second crystalline semiconductor may include depositing an amorphous silicon layer, and crystallizing the amorphous silicon layer by using solid phase crystallization (SPC).

[0027] In an embodiment, the first control electrode and the second control electrode may include a first metal having a higher melting point than a temperature of solid phase crystallization, and the gate line includes a second metal having a lower melting point than that of the first metal.

[0028] According to an embodiment, the protecting member covering the gate line may be formed during the forming of the pixel electrode. The gate line and the pixel electrode may be formed in the same step (concurrently). A voltage assistant line connected to the common electrode may be formed with the gate line and the pixel electrode in the same step (concurrently).

[0029] A method for manufacturing an OLED display according to another exemplary embodiment of the present invention includes: depositing a first metal layer on a substrate; patterning the first metal layer by photolithography to form a control electrode; depositing an amorphous semiconductor on the control electrode; crystallizing the amorphous semiconductor; forming an insulating layer having a contact hole on the crystallized semiconductor; depositing a second metal layer on the insulating layer; and patterning the second metal layer by photolithography to form a gate line connected to the control electrode through the contact hole, wherein the first metal layer has a higher melting point than a temperature for crystallizing the amorphous semiconductor, and the second metal layer has a lower melting point than that of the first metal layer. A pixel electrode separated from the gate line may be formed during the forming of the gate line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. 1 is an equivalent circuit diagram of an OLED display according to an exemplary embodiment of the present invention,

[0031] FIG. 2 is a layout view of an OLED display according to an exemplary embodiment of the present invention,

[0032] FIG. 3 is a cross-sectional view of the OLED display shown in FIG. 2 taken along the line III-III,

[0033] FIG. 4, FIG. 6, FIG. 8, FIG. 10, FIG. 12, and FIG. 14 are layout views sequentially showing processes for manufacturing the OLED display shown in FIG. 2 and FIG. 3 according to an exemplary embodiment of the present invention,

[0034] FIG. 5 is a cross-sectional view of the OLED display shown in FIG. 4 taken along the line V-V,

[0035] FIG. 7 is a cross-sectional view of the OLED display shown in FIG. 6 taken along the line VII-VII,

[0036] FIG. 9 is a cross-sectional view of the OLED display shown in FIG. 8 taken along the line IX-IX,

[0037] FIG. 11 is a cross-sectional view of the OLED display shown in FIG. 10 taken along the line XI-XI,

[0038] FIG. 13 is a cross-sectional view of the OLED display shown in FIG. 12 taken along the line XIII-XIII,

[0039] FIG. 15 is a cross-sectional view of the OLED display shown in FIG. 14 taken along the line XV-XV,

[0040] FIG. 16 is a layout view of an OLED display according to another exemplary embodiment of the present invention,

[0041] FIG. 17 is a cross-sectional view of the OLED display shown in FIG. 16 taken along the line XVII-XVII,

[0042] FIG. 18, FIG. 20, FIG. 22, and FIG. 24 are layout views sequentially showing processes for manufacturing the OLED display shown in FIG. 16 according to another exemplary embodiment of the present invention,

[0043] FIG. 19 is a cross-sectional view of the OLED display shown in FIG. 18 taken along the line XIX-XIX,

[0044] FIG. 21 is a cross-sectional view of the OLED display shown in FIG. 20 taken along the line XXI-XXI,

[0045] FIG. 23 is a cross-sectional view of the OLED display shown in FIG. 22 taken along the line XXIII-XXIII, and

[0046] FIG. 25 is a cross-sectional view of the OLED display shown in FIG. 24 taken along the line XXV-XXV.

DETAILED DESCRIPTION

[0047] Embodiments of the present invention will be described more fully hereinafter with reference to the accompanying drawings. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0048] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Exemplary Embodiment 1

[0049] Now, an OLED display according to an embodiment of the present invention will be described in detail with reference to FIG. 1. FIG. 1 is an equivalent circuit diagram of an OLED display according to an exemplary embodiment of the present invention.

[0050] Referring to FIG. 1, an OLED display according to the present exemplary embodiment includes a plurality of signal lines 121 (also referred to as "gate lines"), 171 (also referred to as "transmitting data lines"), and 172 (also referred to as "driving voltage lines"), and a plurality of pixels PX connected thereto and arranged substantially in a matrix.

[0051] The signal lines include a plurality of gate lines 121 for transmitting gate signals (or scanning signals), a plurality of data lines 171 for transmitting data signals, and a plurality of driving voltage lines 172 for transmitting a driving voltage. The gate lines 121 extend substantially in a row direction and substantially parallel to each other, and the data lines 171 and

the driving voltage lines 172 extend substantially in a column direction and substantially parallel to each other.

[0052] Each pixel PX includes a switching transistor Qs, a driving transistor Qd, a capacitor Cst, and an organic light emitting diode LD. The switching transistor Qs has a control terminal connected to one of the gate lines 121, an input terminal connected to one of the data lines 171, and an output terminal connected to the driving transistor Qd. The switching transistor Qs transmits the data signals applied to the data line 171 to the driving transistor Qd in response to a gate signal applied to the gate line 121.

[0053] The driving transistor Qd has a control terminal connected to the switching transistor Qs, an input terminal connected to the driving voltage line 172, and an output terminal connected to the organic light emitting diode LD. The driving transistor Qd drives an output current I_{LD} having a magnitude that depends on the voltage between the control terminal and the output terminal thereof, and outputs such I_{LD} to the organic light emitting diode LD.

[0054] The capacitor Cst is connected between the control terminal and the input terminal of the driving transistor Qd. The capacitor Cst stores a data signal applied to the control terminal of the driving transistor Qd and maintains the data signal after the switching transistor Qs turns off.

[0055] The organic light emitting diode LD has an anode connected to the output terminal of the driving transistor Qd and a cathode connected to a common voltage Vss. The organic light emitting diode LD emits light having an intensity depending on an output current I_{LD} of the driving transistor Qd, and thereby displays images.

[0056] The switching transistor Qs and the driving transistor Qd may be n-channel field effect transistors (FETs). However, at least one of the switching transistor Qs and the driving transistor Qd may be a p-channel FET. In addition, the connections among the transistors Qs and Qd, the capacitor Cst, and the organic light emitting diode LD may be modified.

[0057] Next, the OLED display shown in FIG. 1 according to an embodiment will be described in detail with reference to FIG. 2, FIG. 3, and FIG. 1. In the present exemplary embodiment, an OLED display of a bottom emission type will be described.

[0058] FIG. 2 is a layout view of an OLED display according to an exemplary embodiment of the present invention, and FIG. 3 is a cross-sectional view of the OLED display shown in FIG. 2 taken along the line III-III.

[0059] A plurality of switching control electrodes 124a and a plurality of driving control electrodes 124b are formed on an insulating substrate 110 made of a material such as transparent glass, plastic, or the like.

[0060] The switching control electrode 124a and the driving control electrode 124b are separated from each other and may be of an island type. According to one or more embodiments, the switching control electrode 124a and the driving control electrode 124b may be made of a refractory metal such as a molybdenum-containing metal including molybdenum (Mo) or a molybdenum alloy (Mo alloy), a chromium-containing metal including chromium (Cr) or a chromium alloy (Cr alloy), a titanium-containing metal including titanium (Ti) or a titanium alloy (Ti alloy), a tantalum-containing metal including tantalum (Ta) or a tantalum alloy (Ta alloy), and a tungsten-containing metal including tungsten (W) or a tungsten alloy (W alloy); however, this is not necessarily limiting.

[0061] According to one or more embodiments, a gate insulating layer 140 may be made of silicon nitride (SiN_x) or silicon oxide (SiO_2) and may be formed on the switching control electrode 124a, the driving control electrode 124b and the insulating substrate 110.

[0062] A plurality of switching semiconductors 154a and a plurality of driving semiconductors 154b may be formed on the gate insulating layer 140. The switching semiconductors 154a and the driving semiconductors 154b may be made respectively of an island type. The switching semiconductors 154a overlap the switching control electrodes 124a, and the driving semiconductors 154b overlap the driving control electrodes 124b. According to an embodiment, the switching semiconductors 154a and the driving semiconductors 154b may be made of a crystallized silicon such as microcrystalline silicon or polycrystalline silicon, but this is not necessarily limiting.

[0063] A plurality of etch stoppers 155a and 155b are respectively formed on the switching semiconductors 154a and the driving semiconductors 154b. The etch stoppers 155a and 155b may be made of silicon nitride, and may protect the switching semiconductor 154a and the driving semiconductor 154b from being damaged.

[0064] A plurality of data lines 171, a plurality of switching output electrodes 175a, a plurality of driving voltage lines 172, and a plurality of driving output electrodes 175b are formed on the etch stoppers 155a and 155b, the switching semiconductors 154a, the driving semiconductors 154b, and the gate insulating layer 140.

[0065] The data lines 171 for transmitting data signals extend substantially in the longitudinal direction. Each data line 171 includes a plurality of switching input electrodes 173a extended toward the switching control electrodes 124a, and an end portion 179 having a large area for contact with another layer or with an external driving circuit. The switching output electrodes 175a are separated from the data lines 171, and are opposite to the switching input electrodes 173a on the switching semiconductors 154a.

[0066] The driving voltage lines 172 for transmitting driving voltages extend substantially in the longitudinal direction. Each driving voltage line 172 includes a plurality of driving input electrodes 173b extending toward the driving semiconductors 154b, and a plurality of storage electrodes 174 overlapping the driving control electrodes 124b. The driving control electrodes 124b overlap the storage electrodes 174 to form storage capacitors Cst.

[0067] The driving output electrodes 175b are separated from the data lines 171, the switching output electrodes 175a, and the driving voltage lines 172, and are opposite to the driving input electrodes 173b on the driving semiconductor 154b.

[0068] The data lines 171, the switching output electrodes 175a, the driving voltage lines 172, and the driving output electrodes 175b may be made of a conductive material having low resistivity.

[0069] A plurality of ohmic contacts 161, 163a, 163b, 165a, and 165b are formed under the data lines 171, the switching output electrodes 175a, the driving voltage lines 172, and the driving output electrodes 175b. According to one or more embodiments, the ohmic contacts 161, 163a, 163b, 165a, and 165b may be made of a material such as silicide or n+ hydrogenated a-Si heavily doped with an n-type impurity

such as phosphorous, or they may be made of microcrystalline silicon or polycrystalline silicon, but this is not necessarily limiting.

[0070] The ohmic contacts 161, 163a, 163b, 165a, and 165b may have substantially the same plane shape as the data lines 171, the switching output electrodes 175a, the driving voltage lines 172, and the driving output electrodes 175b. However, the ohmic contacts 161, 163a, 163b, 165a, and 165b may only be formed between the switching semiconductors 154a and the switching input electrodes 173a, the switching semiconductors 154a and the switching output electrodes 175a, the driving semiconductors 154b and the driving input electrodes 173b, and the driving semiconductors 154b and the driving output electrodes 175b.

[0071] A passivation layer 180 is formed on the data lines 171, the switching output electrodes 175a, the driving voltage lines 172, and the driving output electrodes 175b. The passivation layer 180 has a plurality of contact holes 185a, 185b, 182 respectively exposing the switching output electrodes 175a, the driving output electrodes 175b, and end portions 179 of the data lines 171. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 183 and 184 respectively exposing the switching control electrodes 124a and the driving control electrodes 124b. A plurality of gate lines 121, a plurality of connecting members 85, and a plurality of contact assistant members 86 are formed on the passivation layer 180.

[0072] The gate lines 121 for transmitting gate signals extend substantially in a transverse direction and intersect the data lines 171 and the driving voltage lines 172. The gate lines 121 are connected to the switching control electrodes 124a through the contact holes 183, and include an end portion 129 having a large area for contact with another layer or with an external driving circuit.

[0073] The connecting members 85 connect the switching output electrodes 175a and the driving control electrodes 124b to each other through the contact holes 184 and 185a. The contact assistant members 86 are connected to the driving output electrodes 175b through the contact holes 185b.

[0074] According to one or more embodiments, the gate lines 121, the connecting members 85, and the contact assistant members 86 may be made of a metal having low resistivity such as an aluminum-containing metal including aluminum (Al) or an aluminum alloy (Al alloy), a silver-containing metal including silver (Ag) or a silver alloy Ag alloy, and a copper-containing metal including copper (Cu) or a copper alloy (Cu alloy). These low resistance metals may have a low melting point compared with the refractory metal of the switching control electrodes 124a and the driving control electrodes 124b.

[0075] A plurality of pixel electrodes 191, a plurality of first protecting members 195, second protecting members 196, and contact assistants 82 are formed on the gate lines 121, the connecting members 85, the contact assistant members 86, and the passivation layer 180.

[0076] The pixel electrodes 191 are electrically connected to the driving output electrodes 175b through the contact assistant members 86. The contact assistant members 86 improve the contact characteristic and adhesion between the driving output electrodes 175b and the pixel electrodes 191.

[0077] The first protecting members 195 cover the gate lines 121, and the second protecting members 196 cover the connecting members 85. In an embodiment, the first protecting members 195 and the second protecting members 196

may prevent the gate lines **121** and the connecting members **85** from corroding due to contact with, for example, a chemical solution such as an etchant in the photolithography process of the pixel electrodes **191**.

[0078] The contact assistants **82** are connected to the end portions **179** of the data lines **171** through the contact holes **182**. The contact assistants **82** enhance the adhesion characteristic between the end portions **179** of the data lines **171** and an external device and protect the end portions of the data lines **171**.

[0079] According to one or more embodiments, the pixel electrodes **191**, the first protecting members **195**, the second protecting members **196**, and the contact assistants **82** may be formed of a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO), but this is not necessarily limiting.

[0080] An organic insulating layer **361** is formed on the pixel electrodes **191**, the first protecting members **195**, the second protecting members **196**, the contact assistants **82**, and the passivation layer **180**. The organic insulating layer **361** may have a plurality of openings **365** enclosing the edges of the pixel electrodes **191** like a bank.

[0081] A plurality of light emitting members **370** are formed on the pixel electrodes **191** and are confined in the openings **365**. Each of the light emitting members **370** may have a multi-layered structure including an emitting layer (not shown) for emitting light and auxiliary layers (not shown) for improving the efficiency of light emission of the emitting layer.

[0082] According to one or more embodiments, each of the light emitting members **370** may be made of a low-molecular-weight compound or a high-molecular-weight compound, or a mixture thereof, and uniquely emits light of one primary color such as red, green, and blue.

[0083] The auxiliary layers may include an electron transport layer (not shown) and a hole transport layer (not shown) for improving the balance of electrons and holes, as well as an electron injecting layer (not shown) and a hole injecting layer (not shown) for improving the injection of electrons and holes.

[0084] According to one or more embodiments, the light emitting members **370** may uniquely emit light of one of the primary colors such as red, green, and blue, and may be respectively arranged in each pixel. The light emitting members **370** that emit light of three colors such as red, green, and blue may all be arranged in one pixel with vertical or horizontal deposition to form a white emitting layer under or above the color filters emitting light of one of the primary colors such as red, green, and blue.

[0085] Also, a four-color structure including red, green, blue, and white pixels may be arranged in a stripe or check pattern to improve the luminance as well as the three color structure including red, green, and blue pixels.

[0086] A common electrode **270** is formed on the organic light emitting members **370**. According to one or more embodiments, the common electrode **270** may be disposed on the whole surface of the substrate, and may be formed of an opaque conductive material such as Au, Pt, Ni, Cu, W, or alloys thereof. The common electrode **270** supplies current to the light emitting members **370** in cooperation with the pixel electrodes **191**.

[0087] In the above-described OLED display, the switching control electrode **124a**, which is electrically connected to the gate line **121**, the switching input electrode **173a**, which is

electrically connected to the data line **171**, and the switching output electrode **175a**, form the switching thin film transistor Qs along with the switching semiconductor **154a**. The channel of the switching thin film transistor Qs may be formed in the switching semiconductor **154a** between the switching input electrode **173a** and the switching output electrode **175a**.

[0088] The driving control electrode **124b**, which is electrically connected to the switching output electrode **175a**, the driving input electrode **173b**, which is electrically connected to the driving voltage line **172**, the driving output electrode **175b**, which is connected to the pixel electrode **191**, and the driving semiconductor **154b**, form the driving thin film transistor Qd. The channel of the driving thin film transistor Qd may be formed in the driving semiconductor **154b** between the driving input electrode **173b** and the driving output electrode **175b**.

[0089] A pixel electrode **191**, a light emitting member **370**, and the common electrode **270** form an organic light emitting diode LD having the pixel electrode **191** as an anode and the common electrode **270** as a cathode, or vice versa.

[0090] In the above-described exemplary embodiment of the present invention, the semiconductor of the driving thin film transistor may be made of crystalline silicon such that high carrier mobility and stability for flowing sufficient current to the OLED display may be obtained, thereby improving the brightness of the OLED display. In addition, because the channel of the driving thin film transistor is formed in the crystalline semiconductor, the so-called threshold voltage shift phenomenon that may be caused by applying a constant positive voltage in the driving of an OLED display may be excluded (avoided) such that an image-sticking phenomenon is not generated and a reduction in the life time of the OLED display does not occur.

[0091] Also, in an exemplary embodiment of the present invention, the gate line **121** and the switching control electrode **124a** connected thereto may be formed at different layers and with different materials. That is, the switching control electrode **124a** may be disposed under the switching semiconductor **154a** and may be made of a refractory metal, and the gate line **121** may be disposed on the switching semiconductor **154a** and may be made of a low resistance metal. Accordingly, a control electrode may be disposed under the semiconductor in the bottom gate structure and may be used such that the characteristics of the thin film transistor may be improved.

[0092] On the other hand, in the above-described exemplary embodiment, the crystalline semiconductor may be included to improve the characteristics of the thin film transistor. However, a high temperature crystallization process may be required to form the crystalline semiconductor, and because the control electrode is disposed under the semiconductor in the bottom gate structure, the control electrode may be inevitably exposed to the high temperature crystallization process. Accordingly, in the present exemplary embodiment, the control electrode may be formed of a refractory metal such as a molybdenum-containing metal, a chromium-containing metal, a titanium-containing metal, a tantalum-containing metal, or a tungsten-containing metal, that is, a metal having a higher melting temperature than the temperature for the crystallization of the semiconductor, such that the control electrode is prevented from melting or being thermally damaged in the crystallization process of the semiconductor.

[0093] Also, in an OLED display of a large size, the signal line such as the gate line may be made of a low resistance

metal such as aluminum, copper, or silver so that a signal delay may be prevented. However, because the low resistance metal has a relatively low melting point, it may be melted or may be thermally damaged in the crystallization process. Accordingly, in the present exemplary embodiment, the gate line made of a low resistance metal may be deposited after the completion of the crystallization process such that the low resistance metal is not exposed to a high temperature. The gate line, which may be made of a low resistance metal, may be electrically connected to the control electrode, which may be made of a refractory metal, through the contact hole.

[0094] According to this structure of an embodiment, the desired characteristics of a thin film transistor with a crystalline semiconductor and a bottom gate structure may be obtained and a signal delay may be prevented.

[0095] Next, a method of manufacturing the OLED display shown in FIGS. 2 and 3 according to one or more embodiments will be described with reference to FIGS. 4 to 15 as well as FIGS. 2 and 3.

[0096] FIG. 4, FIG. 6, FIG. 8, FIG. 10, FIG. 12, and FIG. 14 are layout views sequentially showing processes of manufacturing the OLED display shown in FIG. 2 and FIG. 3 according to an exemplary embodiment of the present invention. FIG. 5 is a cross-sectional view of the OLED display shown in FIG. 4 taken along the line V-V. FIG. 7 is a cross-sectional view of the OLED display shown in FIG. 6 taken along the line VII-VII. FIG. 9 is a cross-sectional view of the OLED display shown in FIG. 8 taken along the line IX-IX. FIG. 11 is a cross-sectional view of the OLED display shown in FIG. 10 taken along the line XI-XI. FIG. 13 is a cross-sectional view of the OLED display shown in FIG. 12 taken along the line XIII-XIII, and FIG. 15 is a cross-sectional view of the OLED display shown in FIG. 14 taken along the line XV-XV.

[0097] Referring to FIG. 4 and FIG. 5, a refractory metal (not shown) may be deposited on a substrate 110 and patterned by photolithography to form a plurality of switching control electrodes 124a and a plurality of driving control electrodes 124b.

[0098] Next, referring to FIG. 6 and FIG. 7, a gate insulating layer 140 and an amorphous silicon layer (not shown) may be sequentially deposited on the substrate 110, the switching control electrodes 124a, and the driving control electrode 124b. The amorphous silicon layer may be crystallized. For the crystallization, solid phase crystallization (SPC), rapid thermal annealing (RTA), liquid phase recrystallization (LPR), or excimer laser annealing (ELA) may be used. According to an embodiment, the solid phase crystallization may be used because of its ease in crystallization of a large area. The solid phase crystallization may be executed by heat-treating the amorphous silicon layer for a long time under a temperature of about 500° C. to about 750° C.

[0099] Next, the crystallized silicon layer may be patterned by photolithography to form a plurality of switching semiconductors 154a and a plurality of driving semiconductors 154b with an island shape, for example. Next, a silicon nitride layer may be deposited on the switching semiconductor 154a and the driving semiconductor 154b and may be patterned by photolithography to form a plurality of etch stoppers 155a and 155b.

[0100] Next, referring to FIG. 8 and FIG. 9, an impurity silicon layer (not shown) and a metal layer (not shown) may be sequentially deposited on the gate insulating layer 140, the switching semiconductors 154a, the driving semiconductors 154b, and the etch stoppers 155a and 155b. The metal layer

may be patterned by photolithography to form a plurality of data lines 171 including a plurality of switching input electrodes 173a, a plurality of driving voltage lines 172 including a plurality of driving input electrodes 173b, a plurality of switching output electrodes 175a, and a plurality of driving output electrodes 175b.

[0101] Next, the impurity silicon layer may be etched by using the switching input electrodes 173a, the switching output electrodes 175a, the driving input electrodes 173b and the driving output electrodes 175b as an etch mask to form a plurality of ohmic contacts 163a, 165a, 163b, and 165b substantially having the same shape as the switching input electrodes 173a, the switching output electrodes 175a, the driving input electrodes 173b and the driving output electrodes 175b in plan view. The etch stoppers 155a and 155b prevent the switching semiconductors 154a and the driving semiconductors 154b from being damaged during etching.

[0102] According to an embodiment, a plurality of ohmic contacts 161, 163a, 163b, and 165b may also be formed through the following method. First, an amorphous silicon layer (not shown) may be crystallized, and the etch stoppers 155a and 155b may be formed thereon. Next, the impurity silicon layer (not shown) may be deposited. The crystallized silicon layer and the impurity silicon layer may then be patterned together by photolithography to form a plurality of switching semiconductors 154a and driving semiconductors 154b, and a plurality of ohmic contacts having an island shape, for example. Then, a metal layer may be deposited on the ohmic contact layers and may be patterned by photolithography to form the data lines 171, the driving voltage lines 172, the switching output electrodes 175a, and the driving output electrodes 175b. Next, the ohmic contact layers may be etched by using the switching input electrodes 173a, the switching output electrodes 175a, the driving input electrodes 173b and the driving output electrodes 175b as an etch mask to form a plurality of ohmic contact layers 163a, 165a, 163b, and 165b.

[0103] Referring to FIG. 10 and FIG. 11, a passivation layer 180 may then be formed on the data lines 171, the driving voltage lines 172, the switching output electrodes 175a, the driving output electrodes 175b, and the gate insulating layer 140. The passivation layer 180 and the gate insulating layer 140 may be patterned by photolithography to form a plurality of contact holes 182, 183, 184, 185a, and 185b.

[0104] Next, referring to FIG. 12 and FIG. 13, a low resistance metal layer (not shown) may be deposited on the passivation layer 180, and patterned by photolithography to form a plurality of gate lines 121, a plurality of connecting members 85, and a plurality of contact assistant members 86.

[0105] Referring to FIG. 14 and FIG. 15, an ITO layer may be deposited on the gate lines 121, the connecting members 85, the contact assistant members 86, and the passivation layer 180 and patterned by photolithography to form a plurality of first protecting members 195 covering the gate lines 121, a plurality of second protecting members 196 covering the connecting members 85, a plurality of pixel electrodes 191 disposed on the contact assistant members 86, and a plurality of contact assistants 82 disposed on the end portions 179 of the data lines 171.

[0106] The first protecting members 195 and the second protecting members 196 cover the gate lines 121 and the connecting members 85 such that the first protecting members 195 and the second protecting members 196 may prevent the gate lines 121 and the connecting members 85 from cor-

roding due to contact with, for example, a chemical solution such as an etchant in the photolithography process of the ITO layer.

[0107] Next, referring to FIG. 2 and FIG. 3, an organic insulating layer 361 may be coated on the first protecting members 195, the second protecting members 196, and the pixel electrodes 191, and may be exposed and developed to form a plurality of openings 365.

[0108] Then, a plurality of organic light emitting members 370 including a hole transport layer (not shown) and an emission layer (not shown) may be formed in the openings 365. The light emitting members 370 may be formed by a solution process such as Inkjet printing method or a deposition process using a shadow mask (not shown). According to an embodiment, the Inkjet printing method may be used in which an ink solution is dripped in the opening 365 while moving an Inkjet head (not shown), and a drying process is followed after forming each layer.

[0109] Finally, a common electrode 270 may be formed on the organic insulating layer 361 and the organic light emitting members 370.

Exemplary Embodiment 2

[0110] Next, an OLED display according to another exemplary embodiment of the present invention will be described in detail with reference to FIG. 16 and FIG. 17 as well as FIG. 1.

[0111] An OLED display of the top emission type will be described in the present exemplary embodiment, which may be different from the above-described exemplary embodiment. The overlapping descriptions with the previous exemplary embodiment are omitted, and the same constituent elements are indicated by the same reference numerals.

[0112] FIG. 16 is a layout view of an OLED display according to the present exemplary embodiment, and FIG. 17 is a cross-sectional view of the OLED display shown in FIG. 16 taken along the line XVII-XVII.

[0113] A plurality of switching control electrodes 124a and a plurality of driving control electrodes 124b may be made of a refractory metal, and may be formed on an insulating substrate 110.

[0114] A gate insulating layer 140 may be formed on the switching control electrodes 124a, the driving control electrodes 124b and the insulating substrate 110, and a plurality of switching semiconductors 154a and a plurality of driving semiconductors 154b may be formed on the gate insulating layer 140 with an island shape, for example.

[0115] A plurality of etch stoppers 155a and 155b may be respectively formed on the switching semiconductors 154a and the driving semiconductors 154b.

[0116] A plurality of ohmic contact layers 161, 163a, 165a, 163b, and 165b, a plurality of data lines 171 including a plurality of switching input electrodes 173a and a plurality of end portions 179, a plurality of driving voltage lines 172 including a plurality of driving input electrodes 173b and a plurality of storage electrodes 174, a plurality of switching output electrodes 175a, and a plurality of driving output electrodes 175b may be formed on the etch stoppers 155a and 155b, the switching semiconductors 154a, the driving semiconductors 154b, and the gate insulating layer 140.

[0117] A passivation layer 180 having a plurality of contact holes 182, 183, 184, 185a, and 185b may be formed on the

data lines 171, the driving voltage lines 172, the switching output electrodes 175a, and the driving output electrodes 175b.

[0118] A plurality of gate lines 121, a plurality of voltage assistant lines 122, a plurality of connecting members 85, a plurality of pixel electrodes 191, and a plurality of contact assistants 82 may be formed on the passivation layer 180.

[0119] The gate lines 121 may include lower gate lines 121p, which may be made of an opaque metal having low resistance such as Al, Cu, or Ag, and upper gate lines 121q, which may be made of a transparent conductive material such as ITO or IZO. The gate lines 121 may be electrically connected to the switching control electrodes 124a through the contact holes 183, and may include a plurality of end portions 129 for connection with another layer or with an external driving circuit.

[0120] The voltage assistant lines 122 transmit a common voltage and may be parallel to the gate lines 121. The voltage assistant lines 122 may also include lower voltage assistant lines 122p, which may be made of an opaque metal having low resistance, and upper voltage assistant lines 122q, which may be made of a transparent conductive material such as ITO or IZO.

[0121] The connecting members 85 may also include lower connecting members 85p, which may be made of an opaque metal having low resistance, and upper connecting members 85q, which may be made of a transparent conductive material such as ITO or IZO.

[0122] The pixel electrodes 191 may be connected to the driving output electrodes 175b through the contact holes 185b, and may include lower pixel electrodes 192, which may be made of an opaque metal having low resistance, and upper pixel electrodes 193, which may be made of a transparent conductive material such as ITO or IZO.

[0123] The contact assistants 82 may include lower contact assistants (not shown), which may be made of an opaque metal having low resistance, and upper contact assistants (not shown), which may be made of a transparent conductive material such as ITO or IZO.

[0124] An organic insulating layer 361 may be formed on the gate lines 121, the voltage assistant lines 122, the connecting members 85, the pixel electrodes 191, and the passivation layer 180. The organic insulating layer 361 may have a plurality of openings 365 exposing the pixel electrodes 191 and a plurality of contact holes 362 exposing the voltage assistant lines 122.

[0125] A plurality of organic light emitting members 370 including auxiliary layers and emission layers may be formed in the openings 365. The organic light emitting members 370 may contact the upper pixel electrodes 193, which may be made of a transparent conductive material such as ITO or IZO in the openings 365. The transparent conductive material such as ITO or IZO has a low difference of work function with respect to the organic light emitting members 370 to thereby improve the moving efficiency of the charges.

[0126] A common electrode 270 may be formed on the organic light emitting members 370. The common electrode 270 may be disposed on the whole surface of the substrate, and may be formed of a transparent conductive such as ITO or IZO for the top emission. The common electrode 270 may be electrically connected to the voltage assistant lines 122 through the contact holes 362.

[0127] As described above with respect to an embodiment, the voltage assistant lines 122 connected to the common

electrode 270 are provided, so even if the common electrode 270 is made of a transparent conductive material having high resistance such as ITO or IZO, the common voltage may be stably applied to the common electrode 270. Accordingly, a drop of the common voltage may be reduced, and the common voltage may be uniformly applied to the whole region of the common electrode 270 such that cross-talk due to a difference in brightness may be reduced.

[0128] In the above exemplary embodiment, the driving voltage line 172 is parallel to the data line 171 and the voltage assistant line 122 is parallel to the gate line 121, but the driving voltage line 172 may be parallel to the gate line 121 and the voltage assistant line 122 may be parallel to the data line 171.

[0129] Next, the manufacturing method of the OLED display shown in FIG. 16 and FIG. 17 according to one or more embodiments will be described in detail with reference to FIG. 18 through FIG. 25 as well as FIG. 16, FIG. 17 and FIG. 4 through FIG. 7.

[0130] FIG. 18, FIG. 20, FIG. 22, and FIG. 24 are layout views sequentially showing processes of manufacturing the OLED display shown in FIG. 16 according to another exemplary embodiment of the present invention. FIG. 19 is a cross-sectional view of the OLED display shown in FIG. 18 taken along the line XIX-XIX. FIG. 21 is a cross-sectional view of the OLED display shown in FIG. 20 taken along the line XXI-XXI. FIG. 23 is a cross-sectional view of the OLED display shown in FIG. 22 taken along the line XXIII-XXIII, and FIG. 25 is a cross-sectional view of the OLED display shown in FIG. 24 taken along the line XXV-XXV.

[0131] Referring to FIG. 18 and FIG. 19, as in the above described exemplary embodiment, the switching thin film transistor part and the driving thin film transistor part are formed. The switching thin film transistor part may include a plurality of switching control electrodes 124a, a plurality of switching semiconductors 154a, a plurality of etch stoppers 155a, a plurality of ohmic contacts 161, 163a, and 165b, a plurality of data lines 171 including a plurality of switching input electrodes 173a, and a plurality of switching output electrodes 175a. The driving thin film transistor part may include a plurality of driving control electrodes 124b, a plurality of driving semiconductors 154b, a plurality of etch stoppers 155b, a plurality of ohmic contacts 163b and 165b, a plurality of driving voltage lines 172 including a plurality of driving input electrodes 173b and a plurality of storage electrodes 174, and a plurality of driving output electrodes 175b.

[0132] Next, referring to FIG. 20 and FIG. 21, a passivation layer 180 may be formed on the data lines 171, the driving voltage lines 172, the switching output electrodes 175a, the driving output electrodes 175b, and the gate insulating layer 140. The passivation layer 180 and the gate insulating layer 140 may be patterned by photolithography to form a plurality of contact holes 182, 183, 184, 185a, and 185b.

[0133] Next, referring to FIG. 22 and FIG. 23, an opaque metal layer (not shown) with low resistance and an ITO layer (not shown) may be sequentially deposited on the passivation layer 180 and patterned by photolithography to form a plurality of gate lines 121 including lower gate lines 121p and upper gate lines 121q, a plurality of voltage assistant lines 122 including lower voltage assistant lines 122p and upper voltage assistant lines 122q, a plurality of connecting members 85 including lower connecting members 85p and upper connecting members 85q, a plurality of pixel electrodes 191 including lower pixel electrodes 192 and upper pixel electrodes 193,

and a plurality of contact assistants 82 including lower contact assistants (not shown) and upper contact assistants (not shown).

[0134] Next, referring to FIG. 24 and FIG. 25, an organic insulating layer 361 may be coated on the gate lines 121, the voltage assistant lines 122, the connecting members 85, and the pixel electrodes 191, and may be exposed and developed to form a plurality of openings 365 exposing the pixel electrodes 191 and a plurality of contact holes 362 exposing the voltage assistant lines 122.

[0135] Next, referring to FIG. 16 and FIG. 17, a plurality of organic light emitting members 370 including a hole transport layer (not shown) and an emission layer (not shown) may be formed in the openings 365.

[0136] Finally, a common electrode 270 may be formed on the organic insulating layer 361 and the organic light emitting members 370.

[0137] While one or more embodiments of this invention have been described, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. An organic light emitting diode (OLED) display comprising:

- a gate line;
- a data line intersecting the gate line;
- a switching thin film transistor connected to the gate line and the data line;
- a driving thin film transistor connected to the switching thin film transistor; and
- a light emitting diode (LED) connected to the driving thin film transistor,

wherein the switching thin film transistor includes

- a control electrode connected to the gate line,
- a crystalline semiconductor overlapping the control electrode, and

an input electrode and an output electrode spaced apart from each other on the crystalline semiconductor,

wherein the control electrode and the gate line are respectively disposed under and on the crystalline semiconductor and include different materials.

2. The OLED display of claim 1, wherein

the gate line includes a metal having a melting point less than that of the control electrode.

3. The OLED display of claim 2, wherein

the gate line includes one selected from an aluminum-containing metal, a copper-containing metal, and a silver-containing metal, and

the control electrode includes one selected from a molybdenum-containing metal, a chromium-containing metal, a titanium-containing metal, a tantalum-containing metal, and a tungsten-containing metal.

4. The OLED display of claim 2, wherein the light emitting diode (LED) comprises:

- a first electrode connected to the driving thin film transistor;

a second electrode facing the first electrode; and

a light emitting member disposed between the first electrode and the second electrode,

wherein the first electrode is disposed on the same layer as the gate line.

5. The OLED display of claim 4, wherein the first electrode includes a first layer including a metal and a second layer including a transparent conductive material, and the second layer contacts the light emitting member.
6. The OLED display of claim 4, further comprising a voltage assistant line connected to the second electrode and formed on the same layer as the first electrode and the gate line.
7. The OLED display of claim 6, further comprising an organic insulating layer formed on the first electrode, wherein the organic insulating layer has an opening defining the light emitting member and a contact hole exposing the voltage assistant line.
8. The OLED display of claim 2, wherein the light emitting diode (LED) comprises: a first electrode connected to the driving thin film transistor; a second electrode spaced apart from the first electrode; a light emitting member disposed between the first electrode and the second electrode, and a first protecting member formed on a same layer as the first electrode and covering the gate line.
9. The OLED display of claim 8, further comprising a connecting member connecting the driving thin film transistor and the switching thin film transistor, and formed on the same layer as the gate line.
10. The OLED display of claim 9, further comprising a second protecting member formed on the same layer as the first electrode and covering the connecting member.
11. An OLED display comprising: a first control electrode and a second control electrode formed on a substrate; a first crystalline semiconductor and a second crystalline semiconductor formed on the first control electrode and the second control electrode; a first input electrode and a first output electrode spaced apart from each other on the first crystalline semiconductor; a second input electrode and a second output electrode facing each other on the second crystalline semiconductor; an insulating layer formed on the first input electrode, the first output electrode, the second input electrode, and the second output electrode, and having a first contact hole exposing the first control electrode, a second contact hole exposing the first output electrode, a third contact hole exposing the second control electrode, and a fourth contact hole exposing the second output electrode; a gate line formed on the insulating layer and connected to the first control electrode through the first contact hole; a pixel electrode connected to the second output electrode through the fourth contact hole; a common electrode facing the pixel electrode; and a light emitting member disposed between the pixel electrode and the common electrode.
12. The OLED display of claim 11, wherein the gate line includes a metal having a lower melting point than that of the first control electrode.
13. The OLED display of claim 12, wherein the gate line includes one selected from an aluminum-containing metal, a copper-containing metal, and a silver-containing metal, and the first control electrode includes one selected from a molybdenum-containing metal, a chromium-containing metal, a titanium-containing metal, a tantalum-containing metal, and a tungsten-containing metal.
14. The OLED display of claim 12, wherein the gate line and the pixel electrode are formed on the same layer.
15. The OLED display of claim 14, further comprising a connecting member connecting the first output electrode and the second control electrode to each other through the second contact hole and the third contact hole, wherein the connecting member is formed on the same layer as the gate line and the pixel electrode.
16. The OLED display of claim 15, further comprising a voltage assistant line connected to the common electrode, wherein the voltage assistant line is formed on the same layer as the gate line, the pixel electrode, and the connecting member.
17. The OLED display of claim 14, further comprising a voltage assistant line connected to the common electrode, wherein the voltage assistant line is formed on the same layer as the gate line and the pixel electrode.
18. A method for manufacturing an OLED display, comprising: forming a first control electrode and a second control electrode on a substrate; forming a first crystalline semiconductor and a second crystalline semiconductor on the first control electrode and the second control electrode; forming a first input electrode and a first output electrode spaced apart from each other on the first crystalline semiconductor, and forming the second input electrode and the second output electrode facing each other on the second crystalline semiconductor; forming an insulating layer on the first input electrode, the first output electrode, the second input electrode, and the second output electrode; forming a gate line connected to the first control electrode on the insulating layer; forming a pixel electrode on the insulating layer; forming a light emitting member on the pixel electrode; and forming a common electrode on the light emitting member.
19. The method of claim 18, wherein the forming of the first crystalline semiconductor and the second crystalline semiconductor includes depositing an amorphous silicon layer, and crystallizing the amorphous silicon layer by using solid phase crystallization (SPC).
20. The method of claim 19, wherein the first control electrode and the second control electrode include a first metal having a higher melting point than a temperature of solid phase crystallization, and the gate line includes a second metal having a lower melting point than that of the first metal.
21. The method of claim 20, further comprising a protecting member covering the gate line and is formed during the forming of the pixel electrode.
22. The method of claim 20, wherein the gate line and the pixel electrode are formed concurrently.

23. The method of claim **22**, wherein a voltage assistant line connected to the common electrode is formed concurrently with the gate line and the pixel electrode.

24. A method for manufacturing an OLED display, comprising:

depositing a first metal layer on a substrate;
patterning the first metal layer by photolithography to form a control electrode;
depositing an amorphous semiconductor on the control electrode;
crystallizing the amorphous semiconductor;
forming an insulating layer having a contact hole on the crystallized semiconductor;

depositing a second metal layer on the insulating layer; and
patterning the second metal layer by photolithography to form a gate line connected to the control electrode through the contact hole,

wherein the first metal layer has a higher melting point than a temperature for crystallizing the amorphous semiconductor, and the second metal layer has a lower melting point than that of the first metal layer.

25. The method of claim **24**, wherein a pixel electrode separated from the gate line is formed in the forming of the gate line.

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专利名称(译)	有机发光二极管显示器及其制造方法		
公开(公告)号	US20090121982A1	公开(公告)日	2009-05-14
申请号	US12/239632	申请日	2008-09-26
[标]申请(专利权)人(译)	CHOI JOON HOO 曹圭SIK		
申请(专利权)人(译)	崔俊HOO 曹圭植		
当前申请(专利权)人(译)	崔俊HOO 曹圭植		
[标]发明人	CHOI JOON HOO CHO KYU SIK		
发明人	CHOI, JOON-HOO CHO, KYU-SIK		
IPC分类号	G09G3/30 H01L21/00 H01J1/62		
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摘要(译)

根据一个或多个实施例的有机发光装置包括栅极线，与栅极线交叉的数据线，连接到栅极线和数据线的开关薄膜晶体管，连接到开关薄膜的驱动薄膜晶体管晶体管和连接到驱动薄膜晶体管的发光二极管（LED）。开关薄膜晶体管包括连接到栅极线的控制电极，与控制电极重叠的晶体半导体，以及输入电极和输出电极在晶体半导体上彼此间隔开，其中控制电极和栅极线分别设置在晶体半导体下面和上面，并包括不同的材料。

